深圳市雅创芯瀚电子科技有限公司
SHENZHEN ASTRONG-TECH CO., LTD

AST88E1111BI 单端口

10/100/1000千兆以太网收发器

服务电话：13691641629 13538015750

千兆以太网收发器

概述

AST88E1111BI 是高度集成的千兆以太网物理层收发芯片， 包含一个支持10Base-T/100Base-TX/1000Base-T IEEE 802.3 标准的以太网物理层收发机，和一个支持 1000Base-X IEEE 802.3z 标准的 Serdes 模块。它们提供所有必要的物理层功能，通过 CAT.5 UTP 电缆或光纤发送和接收以太网数据包。AST88E1111BI 采用最先进的 DSP 技术和模拟前端（AFE）技术，可通过 UTP 电缆实现高速数据发送和接收。AST88E1111BI 实现了交叉检测和自动校正，极性校正，自适应均衡， 串扰消除，回声消除，定时恢复和纠错等功能，以提供 10Mbps， 100Mbps 或1000Mbps 下稳定的发送和接收性能。

AST88E1111BI 可以与支持串行千兆媒体独立接口（SGMII）或千兆媒体独立接口（R/G/MII）接口的以太网交换机或 MAC 芯片通信。当使用 SGMII 通信时，通过 SGT±引脚以 1.25 gbaud 差分发送串行数据，并通过 SGR±引脚差分接收串行数据。由于 AST88E1111BI 在 SGMII 输入数据上提供时钟恢复，因此不需要输入时钟。SGMII 接口引脚与 SerDes 接口引脚共用。当使用 R/G/MII 通信时，支持 1.8V、2.5V 或 3.3V 三种接口电平。

应用场景

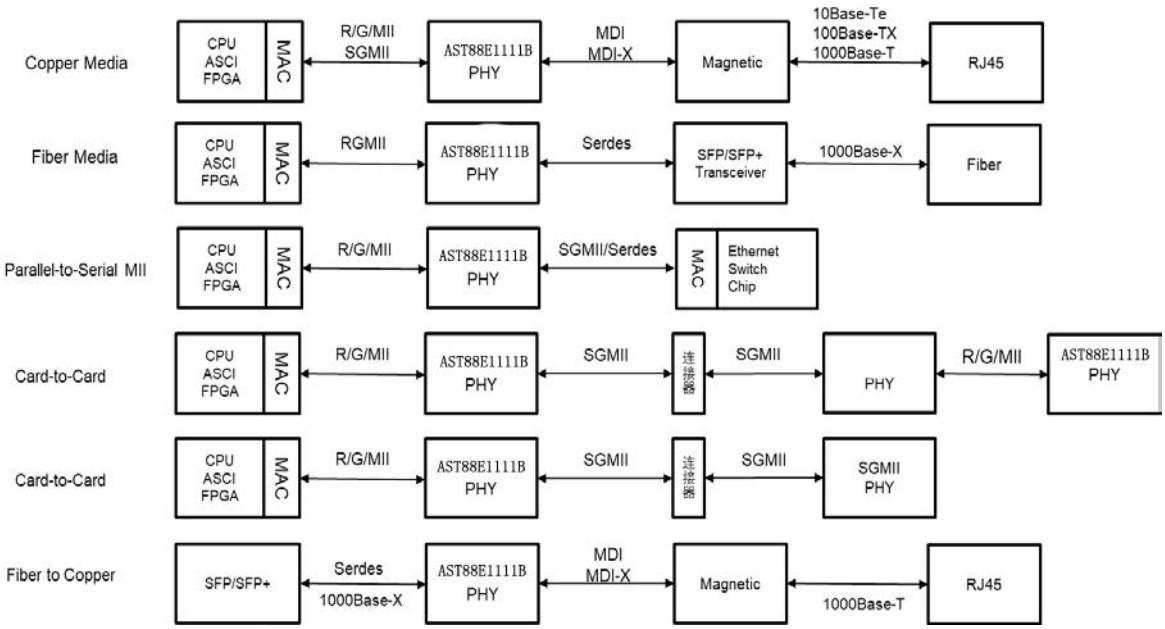
- 数字电视及机顶盒
- 以太网交换机或集线器
- 配合 MAC 芯片的物理层 UTP 连接场景

特性与优势

- 支持 1000Base-T IEEE 802.3ab 标准
- 支持 1000Base-X IEEE 802.3z 标准

- 支持 100Base-TX IEEE 802.3u 标准
- 支持 10Base-T IEEE 802.3 标准
- 支持 2.5V/1.1V 供电
- 支持 1.8/2.5/3.3V R/G/MII 接口
- 支持 SGMII 接口
- 支持 MDI 极性校正
- 支持 MDI 交叉检测及校正
- 1000Base-T 下可支持 100 米五类 UTP 线缆
- 中断输出功能
- 支持 1.8/2.5/3.3V MDIO/MDC 串行管理接口
- LED 状态指示功能
- 支持 25M 或 125M 时钟输入
- BGA-117 封装

应用描述



目　　录

第一章 信号描述

1.1 117-pin BGA 封装

TOPVIEW										
●	1	2	3	4	5	6	7	8	9	
A	RXD5	RXD6	S_IN+	S_IN-	NC	NC	S_OUT+	S_OUT-	LED_LINK1000	A
B	RX_DV	RXD0	RXD3	VDDO	CRS	COL	VDDH	LED_LINK100	VDDH	B
C	RX_CLK	VDDO	RXD2	RXD4	RXD7	DVDD	DVDD	LED_LINK10	LED_RX	C
D	TX_CLK	RX_ER	RXD1	VSS	VSS	VSS	DVDD	CONFIG0	LED_TX	D
E	TX_EN	GTX_CLK	DVDD	VSS	VSS	VSS	DVDD	LED_DUPLEX	CONFIG1	E
F	TXD0	TX_ER	DVDD	VSS	VSS	VSS	VDDH	CONFIG2	CONFIG4	F
G	NC	TXD1	TXD2	VSS	VSS	VSS	CONFIG3	CONFIG6	CONFIG5	G
H	TXD4	TXD3	TXD5	VSS	VSS	VSS	VSS	SEL_FREQ	XTAL1	H
J	TXD6	TXD7	DVDD	VSS	VSS	VSS	DVDD	VDDH	XTAL2	J
K	VDDO	125CLK	RESETn	VSS	VSS	VSS	NC	NC	VDDOX	K
L	INTn	VDDOX	MDC	COMA	VSS	VSS	NC	NC	NC	L
M	MDIO	RSET	VDDH	VDDH	NC	NC	VDDH	VDDH	NC	M
N	MDI[0]+	MDI[0]-	MDI[1]+	MDI[1]-	VDDH	MDI[2]+	MDI[2]-	MDI[3]+	MDI[3]-	N
	1	2	3	4	5	6	7	8	9	

BGA-117 引脚配置（TOP VIEW）

1.2 引脚信号说明

引脚类型定义

引脚类型	定义
IO	输入\输出引脚
I	输入引脚
O	输出引脚
Power	电源引脚
GND	地引脚
NC	悬空引脚
A	模拟信号管脚
D	数字信号管脚

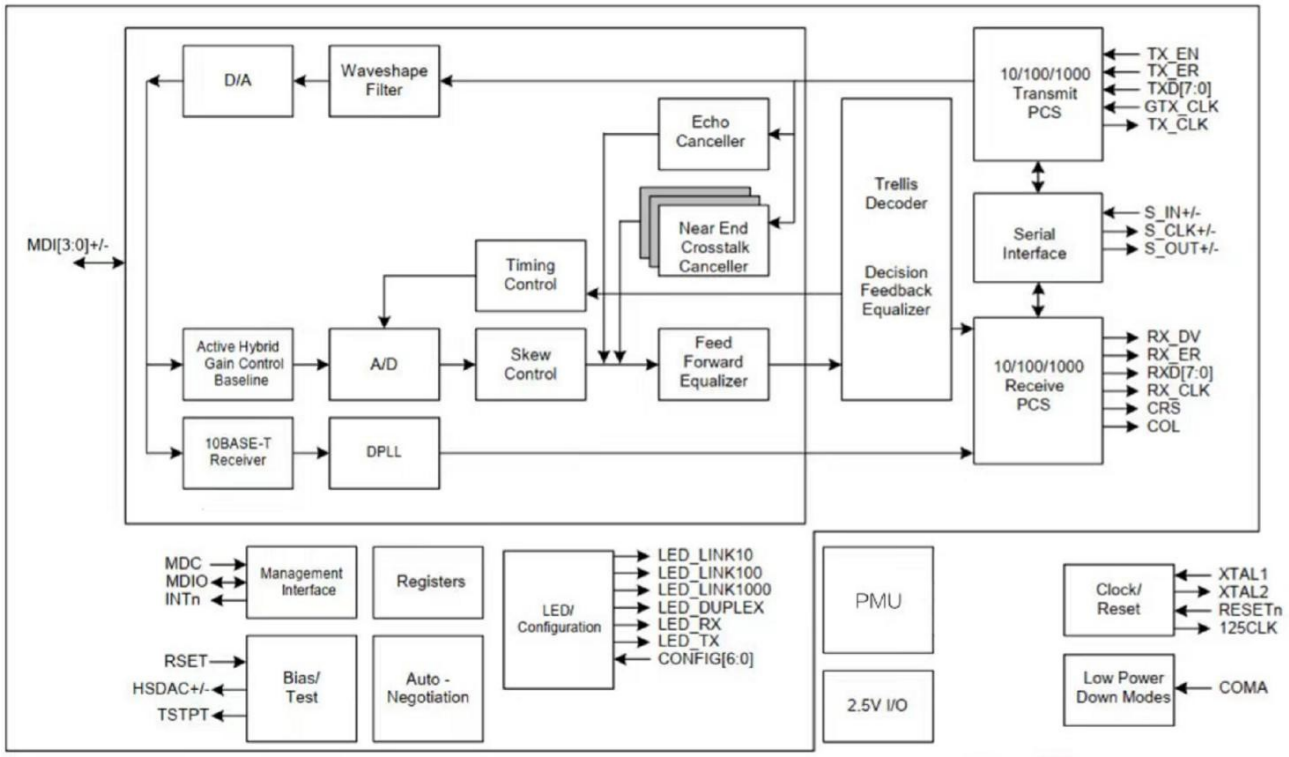
引脚功能描述

引脚编号	名称	类型	描述
MDI 功能引脚			
N1	MDI[0]+	A，IO	在 1000base-T 模式下，四对双绞线同时用于发送和接收数据。 在 10/100base-T 模式下，MDI[0]+、MDI[0]-用于发送数据，而 MDI[1]+、MDI[1]-用于接收数据。 匹配电阻已片内集成。
N2	MDI[0]-	A，IO	
N3	MDI[1]+	A，IO	
N4	MDI[1]-	A，IO	
N6	MDI[2]+	A，IO	
N7	MDI[2]-	A，IO	
N8	MDI[3]+	A，IO	
N9	MDI[3]-	A，IO	
GMII/MII 功能引脚			
E2	GTX_CLK	D，I	为 GMII 发射引脚提供时钟。
D1	TX_CLK	D，O	MII 发射引脚时钟输出。
E1	TX_EN	D，I	GMII/MII 发射使能。
F2	TX_ER	D，I	GMII/MII 发射数据错误指示信号。
J2/J1/H3/H1 H2/G3/G2/F1	TXD[7:0]	D，I	GMII/MII 发射数据总线。
C1	RX_CLK	D，O	GMII/MII 发射引脚时钟输出。
B1	RX_DV	D，O	GMII/MII 接收数据有效性指示。
D2	RX_ER	D，O	GMII/MII 接收数据错误指示信号。
C5/A2/A1/C4 B3/C3/D3/B2	RXD[7:0]	D，O	GMII/MII 接收数据总线。
B5	CRS	D，O	GMII/MII 载波检测信号。
B6	COL	D，O	GMII/MII conllision 检测信号。

RGMII 功能引脚			
E2	TXC	D，I	为 RGMII 发射引脚提供时钟。
H2/G3/G2/F1	TXD[3:0]	D，I	RGMII 发射数据总线。
E1	TX_CTL	D，I	RGMII 发射控制信号。
C1	RXC	D，O	RGMII 发射引脚时钟输出。
B1	RX_CTL	D，O	RGMII 接收控制信号。
B3/C3/D3/B2	RXD[3:0]	D，O	RGMII 接收数据总线。
SGMII 功能引脚			
A3	S_IN+	A，I	SGMII 接收端正极信号输入
A4	S_IN-	A，I	SGMII 接收端负极信号输入
A7	S_OUT+	A，O	SGMII 发送端正极信号输出
A8	S_OUT-	A，O	SGMII 发送端负极信号输出
Serdes 功能引脚			
A3	S_IN+	A，I	1000Base-X 接收端正极信号输入
A4	S_IN-	A，I	1000Base-X 接收端负极信号输入
A7	S_OUT+	A，O	1000Base-X 发送端正极信号输出
A8	S_OUT-	A，O	1000Base-X 发送端负极信号输出
LED 指示功能引脚			
C8	LED_LINK10	D，O	10BASE-T 指示灯
B8	LED_LINK100	D，O	100BASE-T 指示灯
A9	LED_LINK1000	D，O	1000BASE-T 指示灯
E8	LED_DUPLEX	D，O	双工模式指示灯
C9	LED_RX	D，O	接收模式指示灯
D9	LED_TX	D，O	发射模式指示灯
MDIO 配置接口			
L3	MDC	D，I	配置接口时钟输入
M1	MDIO	D，IO	配置接口输入输出数据总线
L1	INTn	D，O	中断功能引脚
其他功能引脚			
K2	125CLK	D，O	为 MAC 芯片提供 125M 时钟
G8/G9/F9/ G7/F8/E9/D8	CONFIG[6:0]	D，I	芯片配置功能引脚
H8	SEL_FREQ	D，I	晶体频率选择引脚
H9/J9	XTAL1/2	A	外接晶体振荡器
K3	RESETn	D，I	芯片复位引脚
L4	COMA	D，I	芯片低功耗使能，拉高有效
M2	RSET	A，I	外接 5K 偏置电阻

电源引脚			
B7/B9/F7/M3/M4/M7/M8/N5/J8	VDDH	POWER	2.5V 电源输入
C2/B4/K1	VDDO	POWER	R/G/MII 接口电源，可支持 1.8/2.5/3.3 多种
K9/L2	VDDOX	POWER	MDC/MDIO/INTn/125CLK/RESETn/COMA 引脚电源，可支持 1.8/2.5/3.3v
C6/C7/D7/E3/E7/F3/J3/J7	DVDD	POWER	芯片 1.1V 内核电源输入
D4/D5/D6/E4/E5/E6/F4/F5/F6/G4/G5/G6/H4/H5/H6/H7 J4/J5/J6/K4/K5/K6/L5/L6	VSS	GND	芯片地电平
NC 引脚			
A5/A6/G1/K7/K8/L7/L8/L9/M5/M6/M9	NC		悬空引脚

第二章 功能描述



AST88E1111BI 功能框图

2.1 接口描述

AST88E1111BI 支持许多数字接口，既支持铜介质，也支持光纤介质。请参阅本节中的连接图。

2.1.1 介质接口

2.1.1.1 铜介质接口

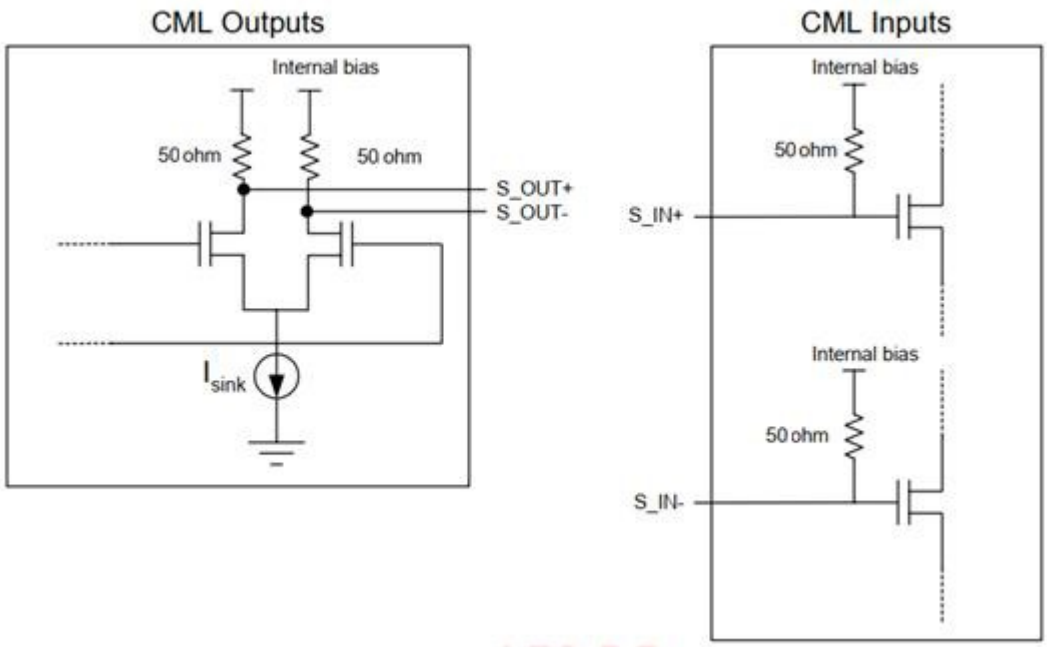
铜介质接口由 MDI[3:0]±引脚组成，引脚可以连接物理介质后可以实现 1000BASE-T、100BASE-TX 和 10BASE-T 的操作模式。MDI 引脚内部已集成阻抗匹配电阻，无需外部配置，直接通过网口变压器接到 RJ-45 连接器上。

2.1.1.2 光纤介质接口

连接到光纤收发器。光纤收发器通过串行接口引脚连接到物理层设备。然后通过 GMII 或 RGMII 接口将 PHY 设备连接到 MAC。串行接口由 S IN±和 S OUT±引脚组成。

SERDES 接口的输入和输出缓冲器内部端接 50 欧姆阻抗，因此不需要外部端接。SERDES 的 I/O 采用

了 CML-buffer。CML 的 IO buffer 可用于连接 PECL 或 LVDS 的 I/O。



2.1.2 MAC 接口

MAC 接口支持 GMII/MII，RGMII 和 SGMII 三种类型，通过这些接口与 MAC 芯片连接。

MAC 接口引脚
GTX_CLK
TX_CLK
TX_ER
TX_EN
TXD[7:0]
RX_CLK
RX_ER
RX_DV
RXD[7:0]
CRS
COL
S_IN±
S_OUT±

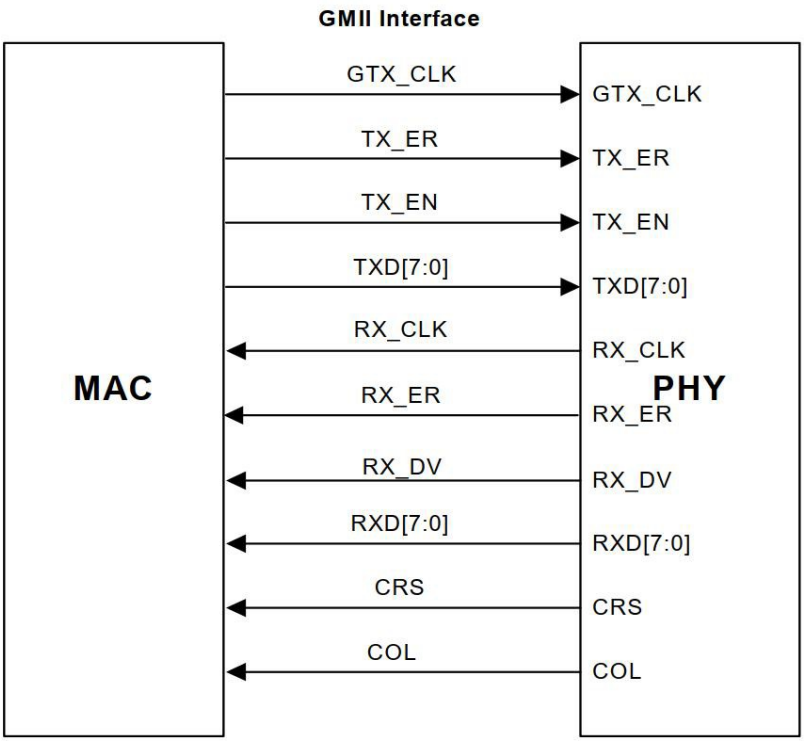
2.2 MAC 接口描述

以下章节描述 MAC 接口的细节。

2.2.1 GMII/MII 接口

GMII/MII 接口的信号如下图所示，其中 MII 通过共享了 GMII 的部分引脚的方式实现 100BASE-TX 和 10BASE-T 模式。通过设置 HWCFG_MODE[3:0] 为 4'b1111，选择 GMII/MII-copper 的通路；设置 HWCFG_MODE[3:0]为 4'b0111，选择 GMII/MII-Fiber 的通路。

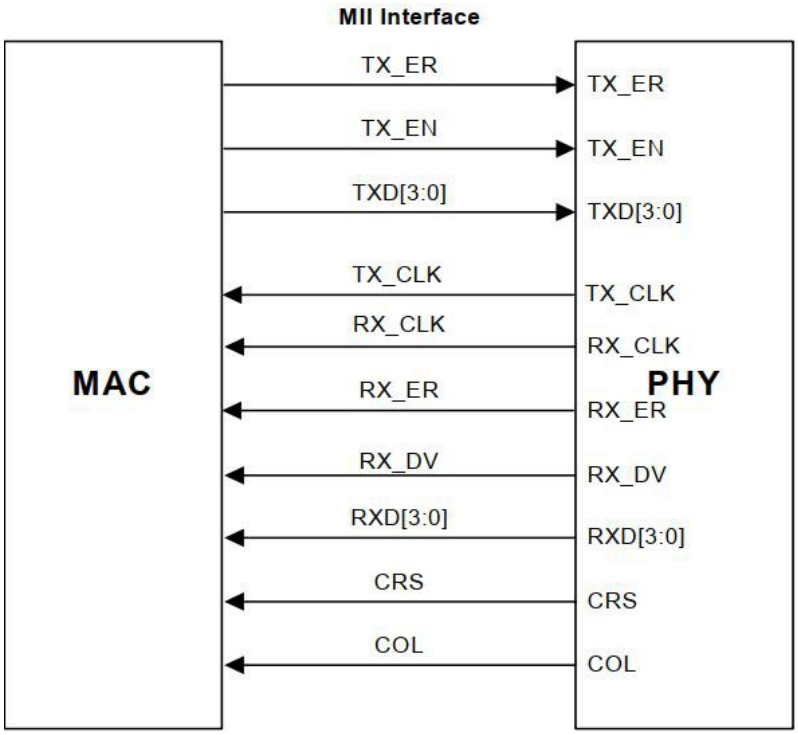
芯片引脚	GMII	MII
GTX_CLK	GTX_CLK	-
TX_CLK	-	TX_CLK
TX_ER	TX_ER	TX_ER
TX_EN	TX_EN	TX_EN
TXD[7:0]	TXD[7:0]	TXD[3:0]
RX_CLK	RX_CLK	RX_CLK
RX_ER	RX_ER	RX_ER
RX_DV	RX_DV	RX_DV
RXD[7:0]	RXD[7:0]	RXD[3:0]
CRS	CRS	CRS
COL	COL	COL



GMII 和 MII 接口分别完全符合 IEEE 802.3 第 35 和 22 条款。GMII 和 MII 接口是通过硬件配置位 HWCFG_MODE[3:0]来使能的，在结束硬件复位时硬件配置位 HWCFG_MODE [3:0]被锁定。请参阅第 xx 页的"硬件配置"。

在 1000BASE-T 模式下，选择 GMII 接口时，TXD[7:0]使用外部输入的 125 MHz 的发送时钟 GTX_CLK，虽然 GTX_CLK 不是 GMII 接口的一部分。同时，TX_CLK 仍然有效，根据寄存器 20 的[6:4]配置值，可以是 25MHz 或 2.5 MHz 或 O MHz。RXD[7:0]使用 125 MHz 的接收时钟 RX_CLK。

在 100BASE-TX 和 10BASE-T 模式下，选择 MII 接口时，TX_CLK 和 RX_CLK 分别源自 25MHz 和 2.5 MHz，分别用于 TXD[3:0]和 RXD[3:0]。此时，GTX_CLK 和 TXD[7:4]信号必须拉高或低，不能悬空（Floating），而 RXD[7: 4]引脚输出低电平。



2.2.2 RGMII 接口

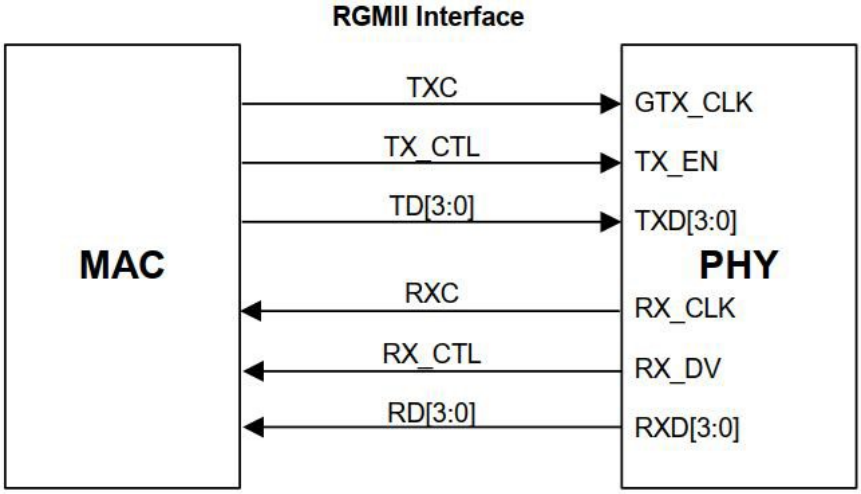
AST88E1111BI 支持 RGMII 规范(2000 年 9 月 22 日的 1.2a 版本，2002 年 4 月的 2.0 版本，虽然不支持 HSTL，但支持 RGMII 版本 2.0 中指定的时序)。不同的 RGMII 时序模型，对时钟和数据之间的时序有不同要求，可以通过设置寄存器 20 的[1]和[7]位进行编程，见第三章寄存器说明。RGMII 接口将 MAC 和 PHY 之间的连接信号减少到了 12 个引脚。减少了数据路径和相关的控制信号，同时对控制信号进行了复用。

通过将 HWCFG_MODE[3:0]位设置为 4'b1011 来选择 RGMII to copper 模式。根据所选择的速度，发射和接收时钟的工作频率分别为 125MHz、25MHz 和 2.5MHz。通过将 HWCFG_MODE[3:0]设置为 4'b0011 来选择 RGMII-Fiber。

当选择 RGMII 模式时，在 GTX_CLK (TXC)的两个时钟边缘上都传输发送控制器信号(TX_CTL)。接收控制在 RX_CLK (RXC)的两个时钟边缘上都传输接收控制器信号(RX_CTL)。

芯片引脚	RGMII 规范对应的引脚	描述
GTX_CLK	TXC	125/25/2.5MHz 的发送时钟，对应速率下可以容忍±50ppm 的误差
TX_EN	TX_CTL	发送控制信号，TX_EN 在 GTX_CLK 的上升沿译码，TX_ER 异或 TX_EN 后在 GTX_CLK 的下降沿译码。
TXD[3:0]	TXD[3:0]	发送数据。 在 1000BASE-T 和 1000BASE-X 模式下，TXD[3:0]在 GTX_CLK 的双沿传输。 在 100BASE-TX 和 10BASE-T 模式下，

		TXD[3:0]只在 GTX_CLK 的上升沿传输。
RX_CLK	RXC	125/25/2.5MHz 的接收时钟，从接收的数据中恢复得到，对应速率下可容忍±50ppm 的误差
RX_DV	RX_CTL	接收控制信号，RX_DV 在 RX_CLK 的上升沿译码，RX_ER 异或 RX_DV 后在 RX_CLK 的下降沿译码。
RXD[3:0]	RXD[3:0]	接收数据。 在 1000BASE-T 和 1000BASE-X 模式下，RXD[3:0]在 RX_CLK 的双沿传输。 在 100BASE-TX 和 10BASE-T 模式下，RXD[3:0]只在 RX_CLK 的上升沿传输。



10/100 Mbps 功能

该接口可用于实现10/100 Mbps 以太网媒体独立接口，作为100 Mbps 时可将时钟频率降低到25 MHz，作为 10 Mbps 操作时可将时钟降低到 2.5 MHz。此时，GTX_CLK (TXC)信号始终由 MAC 生成，RX_CLK (RXC)信号则由 PHY 生成。

在包接收期间，RX_CLK 可以在正脉冲或负脉冲上进行展开，以适应从自由运行的时钟到数据同步时钟域的转换。当物理层的速度改变时，允许对正脉冲或负脉冲进行类似的展开。在速度转换过程中，不允 许出现时钟毛刺。

MAC 必须保持 TX_EN (TX_CTL)为低，直到 MAC 确保 TX_EN (TX_CTL)与 phy 相同的速度运行。

TX ER 和 RX ER 编码

有关 RX_CTL、TX _CTL 和带内编码的定义，请参阅 RGMII 规范。

在 RGMII 模式下，寄存器 20 的[15]位是用来阻止载波扩展的寄存器位。

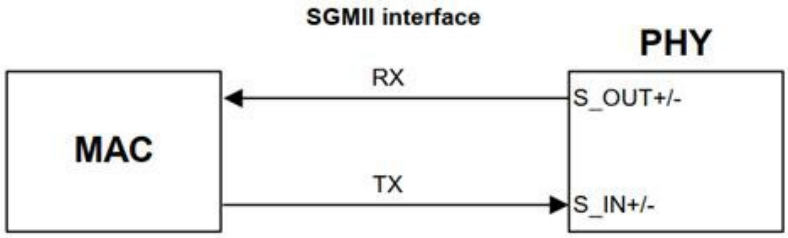
2.2.3 SGMII 接口

AST88E1111BI 支持 SGMII 规范 1.7 版本中的 SGMII-copper 接口，该接口支持 10/100/1000Mbps 的操

作模式。AST88E1111BI 不需要输入 TXCLK，因为 TXCLK 可以从输入的数据中恢复出来。该特性将进一步减少引脚数量、板级的走线，更有利于控制 EMI 和噪声。

在接收侧 AST88E1111BI 仅支持无时钟模式。通过将 HWCFG_MODE[3:0]位设置为 4'b0100 来选择。 对 SGMII 模式来说，如果 bypass 逻辑已经建立了 Fiber 链路，copper 仅在千兆速率下重启自协商。

芯片引脚	SGMII 规范对应引脚	描述
S_OUT±	RX	1.25G 波特率的接收输出，差分
S_IN±	TX	1.25G 波特率的发送输入，差分



2.3 工作模式

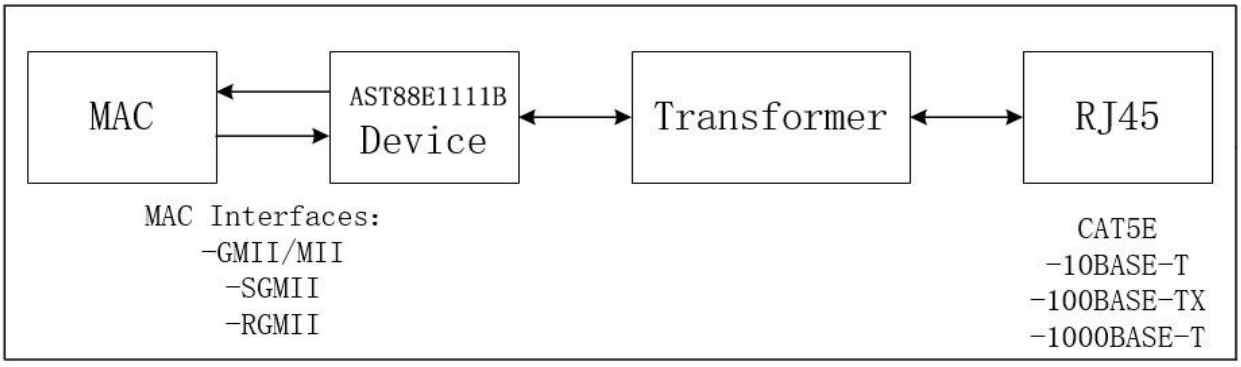
AST88E1111BI 支持下述工作模式，可通过 HWCFG_MODE[3:0]进行配置，对应工作模式配置如下：

工作模式	硬件配置
GMII/MII <-> Copper	HWCFG_MODE[3:0]=1111
GMII <-> Fiber	HWCFG_MODE[3:0]=0111
RGMII<-> Copper	HWCFG_MODE[3:0]=1011
RGMII <-> Fiber	HWCFG_MODE[3:0]=0011
Fiber <-> Copper	HWCFG_MODE[3:0]= 0100
SGMII <-> Copper	HWCFG_MODE[3:0]= 0100
GMII <-> SGMII	HWCFG_MODE[3:0]=1110
RGMII <-> SGMII	HWCFG_MODE[3:0]=0110

其中， Copper 介质支持 10BASE-T 、100BASE-TX 和 1000BASE-T 三种速率； Fiber 介质仅支持 1000BASE-X 速率；SGMII<->Copper 仅支持不带时钟模式；Fiber <-> Copper 详见 2.3.2.3 节。

2.3.1 铜介质操作模式

AST88E1111BI 支持多种 Copper 介质工作模式，如下图所示：



对应工作模式与配置如下:

HWCFG_MODE[3:0]	描述
1111	GMII/MII <-> Copper
1011	RGMI <-> Copper
0100	SGMII <-> Copper

2.3.1.1 GMII/MII-Copper 模式

配置 HWCFG_MODE[3:0]为 4'b1111 可以进入 GMII/MII <-> Copper 工作模式。

2.3.1.2 RGMII-Copper 模式

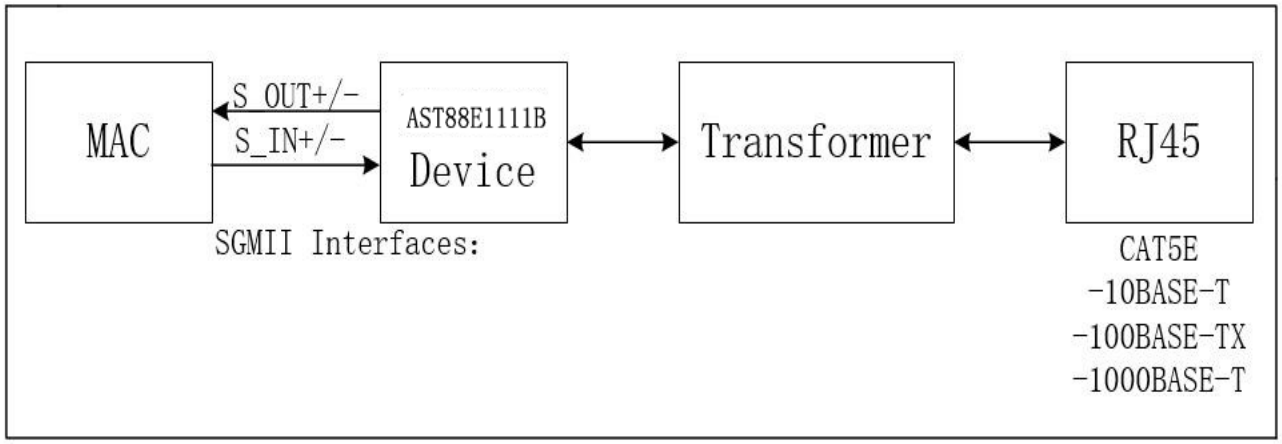
配置 HWCFG_MODE[3:0]为 4'b1011 可以进入 RGMII <-> Copper 工作模式。

2.3.1.3 SGMII-Copper 模式

配置 HWCFG_MODE[3:0]为 4'b0100 可以进入 SGMII <-> Copper 工作模式，该工作模式下 SGMII 接口不支持时钟端口 SCLK+/-。

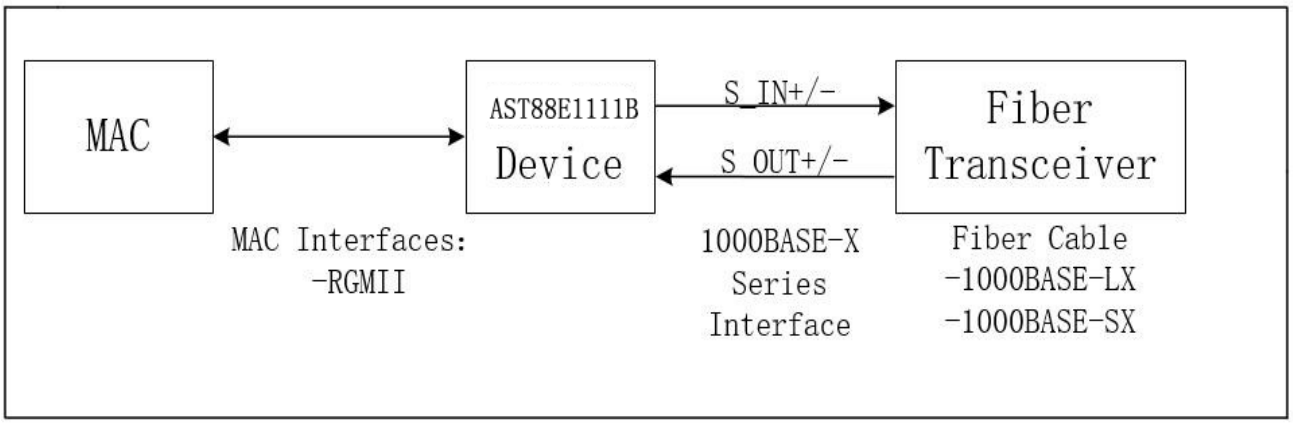
如果 Copper 介质工作在 1000BASE-T 工作模式，1.25GHz 串行端口 SGMII 编码模式与 1000BASE-X 工作模式相同。而在 100BASE-TX 和 10BASE-T 工作模式下，SGMII 接口仍然运行在 1.25GHz 并采用 1000BASE-X 编码，但是，数据包中每个字节会相应重复 10 和 100 次，并在 Transmit 和 Receive 通路上自动使能同步 FIFO。

该工作模式下结构图如下所示:



2.3.2 光纤介质操作模式

AST88E1111BI 支持多种 Fiber 介质工作模式，如下图所示:



对应工作模式与配置如下:

HWCFG_MODE[3:0]	描述
0111	GMII <-> Fiber
0011	RGMI <-> Fiber

2.3.2.1 GMII-Fiber 模式

配置 HWCFG_MODE[3:0]为 4'b0111 可以进入 GMII <-> Fiber 工作模式，该模式下仅支持 1000Mbps 速率，支持自协商。

2.3.2.2 RGMII-Fiber 模式

配置 HWCFG_MODE[3:0]为 4'b0011 可以进入 RGMII <-> Fiber 工作模式，该模式下仅支持 1000Mbps 速率，支持自协商。

2.3.2.3 Fiber-Copper 模式

配置 HWCFG_MODE[3:0]为 4'b0100 可以进入 Fiber<-> Copper 工作模式，该模式下仅支持 1000Mbps 速率；假设本芯片为 A，此通路一般跟另一个处在 RGMII to Fiber 的芯片 B 搭配组成应用方案，请注意:

1、 要求将芯片 B 的 DIS_SLEEP 置 1;

2、 要求将芯片 A 和芯片 B 的 ANEG 配为 4'b1111。

2.3.3 RGMII/GMII->SGMII 操作模式

AST88E1111BI 支持 GMII/RGMII <-> SGMII 工作模式，通过配置 HWCFG_MODE[3:0]为 4'b1110 可以进入 GMII <-> SGMII 工作模式，配置 HWCFG_MODE[3:0]为 4'b0110 可以进入 RGMII <-> SGMII 工作模式，这两种模式均支持 10/100/1000Mbps 速率，SGMII 接口工作在 PHY 模式，与对端 MAC 模式 SGMII 接口对连。在自协商模式下，接收来自 PHY 侧的速率、双工和 link 等自协商信息，待自协商结束后确定速率和双工模式。在上述工作模式下，当自协商完成且 PHY SGMII 的对端 link ok 时 AST88E1111BI 才会 link ok 且使

能对应速率 LED 输出。

如果自协商关闭，速率和双工模式分别由寄存器 20.5:4 和 0_1_8 确定，其中 20.5:4=00/01/10 分别表示 10/100/1000Mbps 速率。

2.3.4 模式切换

由引脚配置的工作模式在复位撤销后可以通过改写寄存器 27.3:0 进行重新配置，任何工作模式改变必须紧跟软复位才会生效。相应的，修改工作模式后需要重新改写下述寄存器：

- 如果从只能工作在 1000Mbps 速率修改至 10/100Mbps 速率工作模式，Copper 介质寄存器 4 必须修改至合适值以广播 10/100Mbps 能力；
- 如果在 SGMII <-> Copper 工作模式和 RGMII <-> Fiber 工作模式间切换，则寄存器 27.12 必须进行相应改写。

2.4 硬件配置

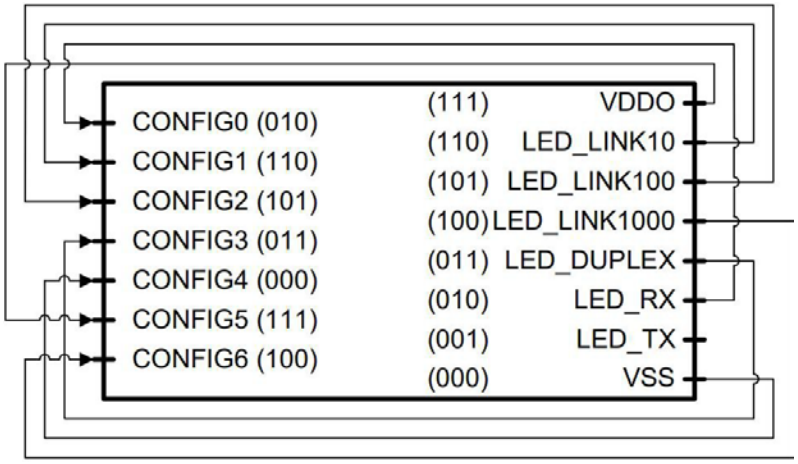
AST88E1111BI 的硬件配置，包括 PHY 地址、工作模式、自协商使能以及物理连接类型等均通过配置引脚CONFIG[6:0]连接至下表中相应引脚进行实现，注意这些 CONFIG[6:0]引脚不能悬空：

引脚	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

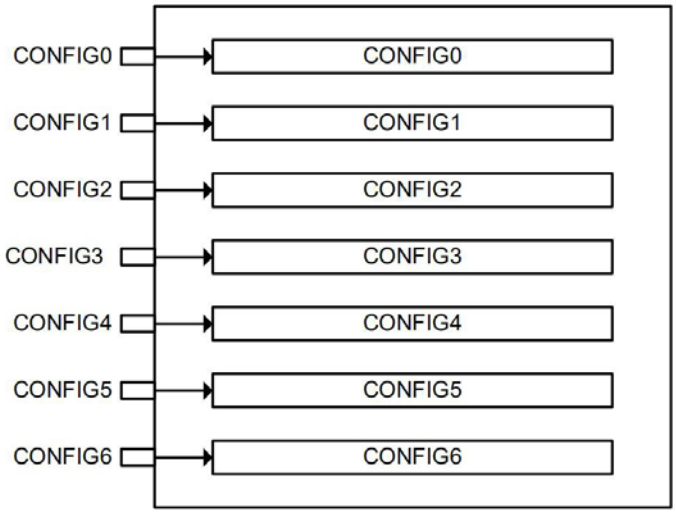
LED 引脚在复位撤销时输出 3 位编码，将 LED 引脚连接到对应 CONFIG 引脚后，CONFIG[6:0]引脚锁存对应三位编码，并进行相应译码，完成对芯片的硬件配置，一个典型的应用配置如下所示：

引脚	LED 引脚连接	配置译码	说明
CONFIG[0]	LED_RX	010	PHY 地址 PHYADR[2:0]=010
CONFIG[1]	LED_LINK10	110	使能 PAUSE，PHYADR[4:3]=10
CONFIG[2]	LED_LINK100	101	自协商使能，仅广播 1000BASE-T 速率，Master 优先
CONFIG[3]	LED_DUPLEX	011	关闭 125CLK 输出
CONFIG[4]	LDE_LINK1000	100	SGMII <-> Copper 工作模式
CONFIG[5]	VSS	000	-
CONFIG[6]	VSS	000	中断信号 INT 高有效

引脚物理连接关系示例如下：



AST88E1111BI 芯片通过在复位撤销时锁存 CONFIG[6:0]引脚的输入对芯片工作模式进行配置，LED 引脚在复位撤销时输出 3 位编码，将 LED 引脚连接到对应 CONFIG 引脚后，CONFIG[6:0]引脚锁存对应三位编码， 并进行相应译码，完成对芯片的硬件配置，如下图所示:



各 CONFIG 引脚对应硬件配置三位译码如下表:

引脚	Bit[2]	Bit[1]	Bit[0]
CONFIG[0]	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG[1]	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG[2]	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG[3]	ANEG[0]	-	DIS_125
CONFIG[4]	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG[5]	Always set to 0	-	HWCFG_MODE[3]
CONFIG[6]	-	INT_POL	-

各硬件配置详细说明如下:

配置	说明
PHYADR[4:0]	PHY 物理地址
ENA_PAUSE	PAUSE 使能 Copper 介质时，0：寄存器 4.11:10 默认值为 00，1：4.11:10 默认值为 11 Fiber 介质时，0：寄存器 4.8:7 默认值为 00，1：4.8:7 默认值为 11

ANEG[3:0]	Copper 介质时自协商配置: 0000: 强制 10BASE-T 半双工 0001: 强制 10BASE-T 全双工 0010: 强制 100BASE-TX 半双工 0011: 强制 100BASE-TX 全双工 1000: 自协商、仅广播 1000BASE-T 全双工，强制 Master 1001: 自协商、仅广播 1000BASE-T 全双工，强制 Slave 1010: 自协商、仅广播 1000BASE-T 全双工，优先 Master 1011: 自协商、仅广播 1000BASE-T 全双工，优先 Slave 1100: 自协商、广播所有速率能力，强制 Master 1101: 自协商、广播所有速率能力，强制 Slave 1110: 自协商、广播所有速率能力，优先 Master 1111: 自协商、广播所有速率能力，优先 Slave 其它：保留
ANEG[3:2]	Fiber 介质时自协商配置: 10: 强制 1000BASE-X 全双工 11：自协商使能 其它：保留
DIS_125	Disable 125MHz clock 0=Enable 125CLK 1=Disable 125CLK
HWCFG_MODE[3:0]	工作模式配置: 0100: Fiber<-> Copper（具体请参考 2.3.2.3 节） 0100: SGMII <-> Copper（自协商使能） 0110: RGMII <-> SGMII 1110: GMII <-> SGMII 0011: RGMII <-> Fiber 0111: GMII <-> Fiber 1011: RGMII <-> Copper 1111: GMII <-> Copper 其它：保留
INT_POL	中断输出极性，0：INTn 引脚中断输出高有效，1：中断输出低有效

2.5 铜缆媒体发送和接收功能

以下各节介绍了 AST88E1111BI 设备的发送和接收路径。

2.5.1 发送端网络接口

多模式 TX 数模转换器

AST88E1111BI 器件集成了多模式发射 DAC，可生成经过滤波的 4D PAM 5，MLT3 或 Manchester 编码符号。发送 DAC 执行信号波形整形以降低 EMI。发送 DAC 设计极低的寄生负载电容，以改善对回波损耗的要

求，从而允许使用低成本变压器。

摆率控制和波形整形

在 1000BASE-T 模式下，使用部分响应滤波和压摆率控制来最小化高频 EMI。 在 100BASE-TX 模式，压摆率控制用于最大程度地减少高频 EMI。 在 10BASE-T 模式下，输出波形通过数字滤波器进行预均衡。

2.5.2 编码器

1000BASE-T

在 1000BASE-T 模式下，发送数据字节被加扰为 9 位符号，并被编码为 4D PAM 5 符号。 初始化后，初始加扰种子由 PHY 地址确定。 这样可以防止多个 AST88E1111BI 器件在空闲期间不会输出相同的序列，这有助于降低 EMI。

100BASE-TX

在 100BASE-TX 模式下，发送数据流经过 4B / 5B 编码，序列化和加密。 初始化后，初始加扰种子由 PHY 地址确定。 这样可以防止多个 AST88E1111BI 器件输出在空闲期间设置相同的顺序，这有助于降低 EMI。

10BASE-T

在 10BASE-T 模式下，发送数据被序列化并转换为曼彻斯特编码。

2.5.3 接收方网络接口

模数转换器

AST88E1111BI 器件在每个接收通道上都集成了先进的高速 ADC，其分辨率高于 802.3ab 标准委员会参考模型中使用的 ADC。 分辨率更高的 ADC 可以带来更好的 SNR，因此可以降低错误率。 该电路架构和设计技术可实现高差分和积分线性，高电源噪声抑制以及低亚稳态错误率。 ADC 以 125 MHz 采样输入信号。

驱动电路

AST88E1111BI 器件采用了先进的片上驱动电路，可显着降低近端回声，即在接收信号上叠加的发射信号。混合器将回声减至最小，以降低数字回声消除器的精度要求。片上驱动电路允许发送器和接收器使用相同的变压器耦合到双绞线电缆，从而降低了整个系统的成本。

回声消除器

由于跳线阻抗不匹配，跳线面板不连续以及沿双绞线电缆的电缆阻抗变化，残留回波无法被混合信号 和回波消除，从而导致接收信号的 SNR 急剧下降。 AST88E1111BI 设备采用了全面开发的数字回声消除器，可以针对 100 多米电缆的回声衰减进行调整。回波消除器具有完全自适应性，可以补偿信道条件随时间的变化。

NEXT 消除器

???1000BASE-T 物理层使用所有 4 对线来传输数据，以将波特率要求降低到仅 125 MHz。这导致在同一束中的相邻电缆对之间产生明显的高频串扰。AST88E1111BI 器件在每个接收通道上使用3 个并行NEXT 消除

器，以消除任何高频信号。

相邻 3 个发射器引起的频率串扰。完全自适应的数字滤波器用于补偿信道条件的时变特性。

基线漂移消除器

与传统的 100BASE-TX 环境相比，在 1000BASE-T 环境中基线漂移问题更大，这是由于发送和接收信号中的 DC 基线偏移所致。 AST88E1111BI 器件采用高级基线漂移消除电路来自动补偿该 DC 偏移。它最小化 DC 基线偏移对整体错误率的影响。

数字自适应均衡器

数字自适应均衡器消除了接收机处的符号间干扰。数字自适应均衡器从 ADC 输出中获取未均衡的信号，并结合使用前馈均衡器（FFE）和判决反馈均衡器（DFE）以获得最佳优化的信噪比（SNR）。

数字锁相环

在 1000BASE-T 模式下，从发送器必须使用在接收信号上看到的确切接收时钟频率。从属发射机必须跟踪并重复接收信号上的任何轻微的长期频率相位拟合（频率漂移）；否则，从属物理层设备和主物理层 设备的接收器都具有难以消除回声和 NEXT 分量。在 AST88E1111BI 器件中，高级 DPLL 用于从接收信号中恢复和跟踪时钟时序信息。该 DPLL 本身具有非常低的长期相位发射器，从而使 SNR 可达到最大化。

2.5.4 解码器

1000BASE-T

在 1000BASE-T 模式下，将分析接收的空闲流，以便可以确定扰码器的种子，4 对信号时钟的偏斜，以 MDI 线序和极性。校准后，将 4D PAM 5 符号转换为 9 位符号，然后将其解扰为 8 位数据值。如果解扰器由于任何原因失去锁定，则在自动协商完成后，将断开链路并重新开始校准。

100BASE-TX

在 100BASE-TX 模式下，将恢复接收数据流并将其转换为 NRZ。 NRZ 被解码并与符号边界对齐。然后将对齐的数据并行化并解码 5B / 4B。除非扰码器被锁定，否则接收器不会尝试对数据流进行解码。在检测到足够数量的连续空闲代码组之后，解扰器“锁定”到扰码器状态。一旦锁定，解扰器将连续监视数据流， 以确保它没有丢失同步。当检测到链路故障情况或检测到不足的空闲符号时，解扰器总是被强制进入解锁状态。

10BASE-T

在 10BASE-T 模式下，恢复的 10BASE-T 信号从曼彻斯特解码为 NRZ，然后对齐。必须进行对齐以确保帧定界符（SFD）的起始位置对齐半字节边界。

2.6 电源

AST88E1111BI 芯片需要两种电源供电：VDDH 电源域和 DVDD 电源域，供电电压分别为 2.5V 和 1.1V。 IO 电源为两个独立的分组：VDDO，VDDOX，IO 电源域支持 1.8V/2.5V/3.3V 三种电压，根据实际情况需要给 IO 电源域配置对应电压。

2.6.1 VDDO 电源域

VDDO 用于为 MAC 接口 IO 供电。 VDDO 支持三种电源选项：1.8V/2.5V/3.3V。

2.6.2 VDDOX 电源域

VDDOX 用于 MDC / MDIO / INTn / 125CLK / RESETn 引脚电源。VDDOX 支持三种电源选项：1.8V/2.5V/3.3V。

2.6.3 VDDH 电源域

VDDOH 主电源用于其他数字 IO 电源和模拟电路电源。 VDDH 支持 2.5V。

2.6.4 DVDD 电源域

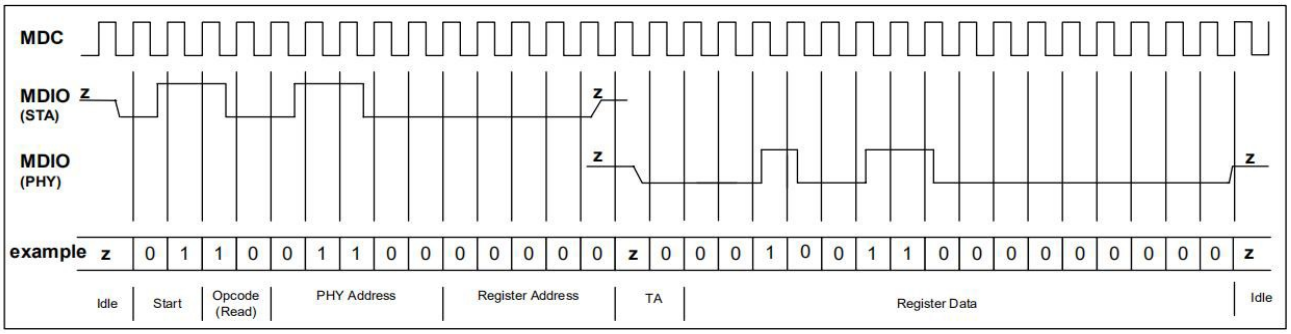
DVDD 电源主要用于其它数字/模拟逻辑电路电源。 DVDD 支持 1.1V，使用 1.0 V or 1.2V 也均正常。

2.7 管理接口

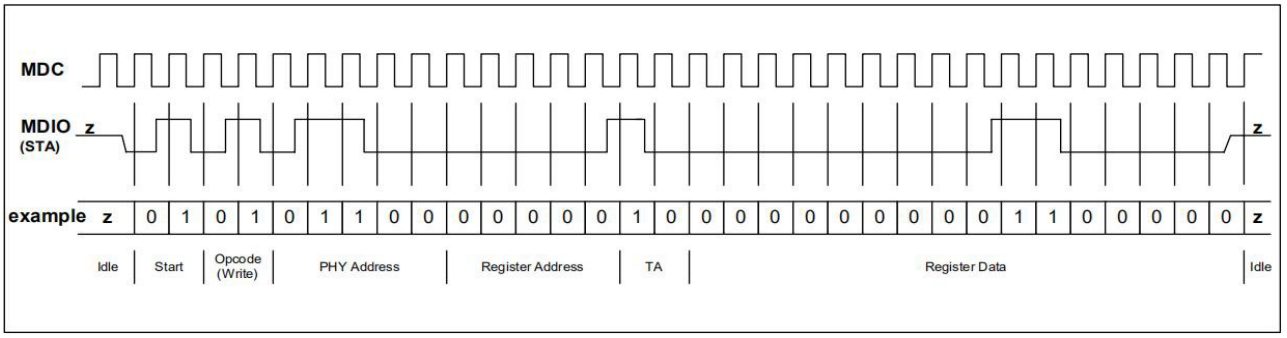
管理接口提供通过 MDC/MDIO 引脚访问内部寄存器功能，兼容 IEEE802.3u 的 Clause22 协议，MDC 为管理时钟输入，最高支持 8.3MHz，MDIO 引脚为双向数据传输引脚，同步于 MDC 时钟。MDIO 引脚需要外部上拉，上拉电阻为 1.5k~10k 欧姆。

管理接口对应的 PHY 物理地址由引脚硬件配置 PHYADR[4:0]确定，详见硬件配置章节说明。

典型的管理接口读内部寄存器时序说明如下：



典型的管理接口写内部寄存器时序说明如下：



串行管理接口协议说明如下:

32bit 前导码（全 1）	起始码	操作码 10 读/01 写	5bit PHY 物理地址	5bit 寄存器地址	2bit 翻转码 z0 读/10 写	16bit 数据	空闲码
1111…1111	01	10	01100	00000	z0	0001….0000	111111

MDC/MDIO 协议仅支持 32 个寄存器，AST88E1111BI 采用页扩展方式支持寄存器扩展，比如寄存器 29 用于寄存器 30 的页扩展，而其他寄存器的页扩展由寄存器 22 指定，详见寄存器章节说明。AST88E1111BI 寄存器访问支持不带前导码，即 32bit 全 1 访问方式。

2.8 自协商功能

AST88E1111BI 支持 3 种类型的自协商:

1) 10/100/1000BASE-T 铜介质自协商（IEEE 802.3 第 28 章和第 40 章）
2) 1000BASE-X 自协商（IEEE 802.3 第 37 章）
3) SGMII 自协商

自协商机制可以实现本地与链路对端设备实现能力交换，包括链路速率、双工模式、Master/Slave 模式等。

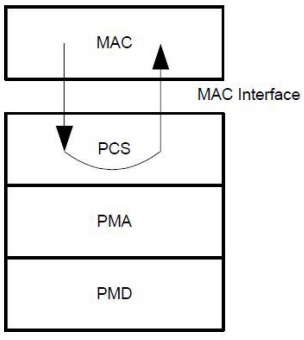
1000BASE-X 仅支持 1000Mbps 速率。

自协商发生在以下时机:

1) 硬件复位
2) 软件复位（寄存器 0.15）
3) 重启自动协商（寄存器 0.9）
4) 从 power down 到 power up（寄存器 0.11）

2.9 自环模式

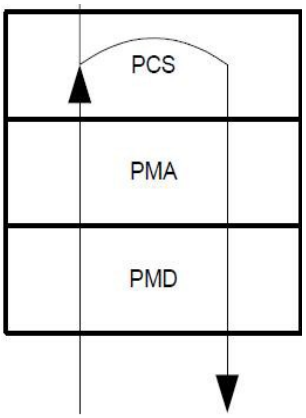
2.9.1 PCS 自环



PCS 自环

光纤和铜介质模式时，都支持 PCS 自环，通过配置寄存器 0.14 实现。设备处于 PCS 自环模式时，从 MAC 接口收到的包在 PCS 层环回，返回到 MAC 接口。

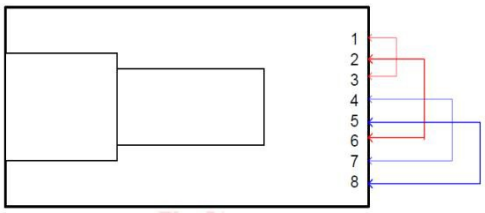
2.9.2 远端自环



远端自环

100BASE-T 模式时，支持远端自环，从底层链路收到包时，在 PCS 层环回至链路。远端自环通过配置寄存器 20.14 实现。

2.9.3 外部自环



外部自环

10/100BASE-T 模式时，支持外部自环，从 MAC 接收收到的包，传至底层链路，再从底层链路环回，介质在物理上需要自环连线。

2.10 MDI/MDIX 交叉

AST88E1111BI 设备支持自动识别介质线缆是否需要交叉，即支持 MDI/MDIX 模式自动识别。寄存器 17.6 记录了 MDI/MDIX 状态，寄存器 28[5:0]（Page 5）记录了 A/B/C/D 各通道的交叉状态。

MDI/MDIX 状态对应的 Pin 映射如下表所示。

Pin	MDI			MDIX		
	1000BASE-T	100BASE-T	10BASE-T	1000BASE-T	100BASE-T	10BASE-T
MDI[0]+-	BI_DA+-	TX+-	TX+-	BI_DA+-	RX+-	RX+-
MDI[1]+-	BI_DB+-	RX+-	RX+-	BI_DB+-	TX+-	TX+-
MDI[2]+-	BI_DC+-			BI_DC+-		
MDI[3]+-	BI_DD+-			BI_DD+-		

2.11 极性校准

AST88E1111BI 设备支持在接收端自动极性校准，当接收器的解码器锁定时，各通道的极性也被锁定。极性状态在寄存器 17.1 中记录。寄存器 28[3:0]（Page 5）记录了 A/B/C/D 各通道的极性翻转状态。

2.12 LED 接口

LED 接口包含 LED_LINK10、LED_LINK100、LED_LINK100、LED_DUPLEX、LED_RX 和 LED_TX 共 6 根输出引脚，支持手动控制（与内部功能和状态无关，通过改写内部寄存器 25 实现）。每个 LED 引脚可以独立控制，比如每个 LED 引脚可以选择手动控制输出，而其他引脚由内部工作状态确定输出。

2.12.1 手动控制输出

与 PHY 的工作状态无关，每个 LED 引脚输出均可以被手动控制，比如关闭、打开或者闪烁，通过改写寄存器 25 的[11:0]实现，分别控制 6 个 LED 引脚输出，详细说明如下：

寄存器 25	对应 LED
[11:10]	LED_DUPLEX
[9:8]	LED_LINK10
[7:6]	LED_LINK100
[5:4]	LED_LINK1000
[3:2]	LED_RX
[1:0]	LED_TX

比如 LED_TX 引脚对应控制位为寄存器 25.1:0，对应配置说明如下：

1） 2'b00: 默认为 Normal 模式，该 LED 引脚由寄存器 24 配置根据 PHY 工作状态输出；

2） 2'b01: Blink，该 LED 引脚根据寄存器 24 配置 blink rate 进行 01 周期性闪烁；

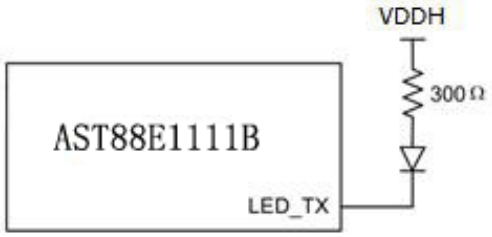
3） 2'b10: 关断，LED 引脚输出高电平；

4） 2'b11: 打开，LED 引脚输出低电平。

因此，各 LED 引脚仅在寄存器 25 对应配置位为 2'b00 时工作在普通模式，由寄存器 24 配置以及 PHY 工作状态进行控制输出。

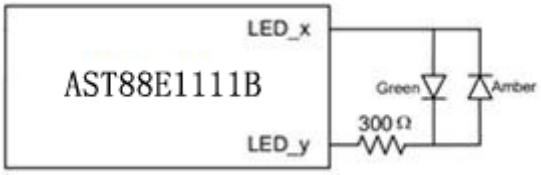
2.12.1.1 LED 连接方式

LED 灯可以采用单色 LED 或者双色 LED 模式，单色 LED 使用结构如下图所示，LED 输出为低有效，LED 灯正极采用 300 欧姆电阻上拉至 VDDH，负极直接连接至 LED 引脚。



双色 LED 使用结构如下图所示，任何两个 LED 引脚输出可以用来实现双色 LED 灯，两个 LED 引脚功能独立，通过组合产生双色显示，比如，绿色 Green LED 灯亮表示 100Mbps 速率，而黄褐色 Amber LED 灯亮表示 1000Mbps 速率，则可以连接如下：

- LED_LINK1000 引脚连接到黄褐色 Amber LED 灯的负极（LED_x）；
- LED_LINK100 引脚连接到绿色 Green LED 灯的负极（LED_y）。



2.12.2 功能性 LED

LED 功能由 PHY 的工作状态进行控制，区别于手动控制输出。每个 LED 引脚可以用于表示多种 PHY 状态以及不同闪烁频率，包含 4 类 LED：直接 LED 模式和 3 类组合 LED 模式。

2.12.2.1 直接驱动 Link LED 模式

当寄存器 24.5:3 为 3'b000 时，LED 输出为直接 LED 模式，具体如下：

LED 输出引脚	LED 输出说明
LED_LINK10	低：10Mbps 速率链路 link up 高：10Mbps 速率链路 link down
LED_LINK100	低：100Mbps 速率链路 link up 高：100Mbps 速率链路 link down
LED_LINK1000	低：1000Mbps 速率链路 link up 高：1000Mbps 速率链路 link down

2.12.2.2 组合 Link LED 模式

有 3 种组合 Link LED 模式，当寄存器 24.5:3 为 3'b011 时，Link LED 输出具体如下：

LED 输出引脚			速率	Link 状态
LED_LINK1000	LED_LINK100	LED_LINK10		
高	高	高	任意速率	Link down
高	高	低	10Mbps	Link up
高	低	高	100Mbps	Link up
低	高	高	1000BASE-T(Slave)	Link up

低	高	低	1000BASE-T(Master)	Link up
低	高	高	1000BASE-X	Link up

当寄存器 24.5:3 为 3'b001 时，LED_LINK1000 引脚用于全局 Link 显示，Link LED 输出具体如下：

LED 输出引脚			速率	Link 状态
LED_LINK1000	LED_LINK100	LED_LINK10		
低	低	低	1000Mbps	Link up
低	低	高	100Mbps	Link up
低	高	低	10Mbps	Link up
高	高	高	任意速率	Link down

当寄存器 24.5:3 为 3'b010 时，LED_LINK10 引脚用于全局 Link 显示，Link LED 输出具体如下：

LED 输出引脚			速率	Link 状态
LED_LINK1000	LED_LINK100	LED_LINK10		
低	高	低	1000Mbps	Link up
高	低	低	100Mbps	Link up
高	高	低	10Mbps	Link up
高	高	高	任意速率	Link down

当寄存器 24.5:3 为 3'b100 时，Link LED 输出具体如下：

LED 输出引脚			速率	Link 状态
LED_LINK1000	LED_LINK100	LED_LINK10		
低	高	高	1000Mbps Link 且 " RGMII <-> 1000BASE-X 模式	Link up
高	低	高	100Mbps	Link up
高	高	低	10Mbps	Link up
高	高	高	任意速率	Link down

当寄存器 24.5:3 为 3'b111 时，Link LED 输出具体如下：

LED 输出引脚			速率	Link 状态
LED_LINK1000	LED_LINK100	LED_LINK10		
低	低	高	1000Mbps Link(1000BASE-X)	Link up
低	高	低	1000BASE-T(Master)	Link up
低	高	高	1000BASE-T(Slave)	Link up
高	低	高	100Mbps	Link up
高	高	低	10Mbps	Link up
高	高	高	任意速率	Link down

2.12.2.3 DUPLEX/RX 和 TX LED 模式

LED_DUPLEX 输出如下：

寄存器 24.2	寄存器 24.7	LED_DUPLEX 输出说明
0	0	低：全双工 高：半双工 闪烁：Collision
1	0	低：全双工 高：半双工
0	1	低：Fiber link up 高：Fiber link down
1	1	保留

LED_RX 输出如下：

寄存器 24.1	LED_RX 输出说明
0	低：Link up 高：Link down 闪烁：正在接收包
1	低：正在接收包 高：未接收包

LED_TX 输出如下：

寄存器 24.6	寄存器 24.0	LED_TX 输出说明
0	0	低：正在发送包 高：未发送包
0	1	低：Link up 高：Link down 闪烁：正在传输包
1	0	低：正在传输包 高：未传输包
1	1	高：未传输包 闪烁：正在传输包

2.12.2.4 LED 脉冲延展和闪烁

部分 LED 输出状态持续时间可能很短，在 LED 灯上难以观测，可以进行脉冲延展，扩宽 LED 脉冲以便 LED 观测。脉冲延展宽度由寄存器 24.14:12 进行配置，默认值为 170~340ms。脉冲拉伸持续时间仅适用于 LED_DUPLEX 的 collision 模式、LED_RX 和 LED_TX 引脚输出的 Link、速率和双工模式。

部分状态可以通过 LED 闪烁进行显示，闪烁周期由寄存器 24.10:8 进行配置，默认闪烁周期为 84ms。闪烁频率仅适用于 LED_DUPLEX 的 collision 模式、LED_RX 和 LED_TX 引脚输出的 Link、速率和双工模式

第三章 寄存器描述

3.1 概述

AST88E1111BI 芯片寄存器实现统计概况如下:

寄存器序号	Page0(Copper)	Page1(Fiber)
0	Control Register	Control Register
1	Status Register	Status Register
2	PHY Identifier	
3	PHY Identifier	
4	Auto-Neg Advertisement Register	Auto-Neg Advertisement Register
5	Link Partner Ability Register	Link Partner Ability Register
6	Auto-Neg Expansion Register	Auto-Neg Expansion Register
7	Next Page Transmit Register	Next Page Transmit Register
8	Link Partner Next Page Register	Link Partner Next Page Register
9	1000BASE-T Control Register	
10	1000BASE-T Status Register	
11	Reserved Register	
12	Reserved Register	
13	Reserved Register	
14	Reserved Register	
15	Extended Status Register	
16	PHY Specific Control Register	
17	PHY specific Status Register	PHY specific Status Register
18	Interrupt Enable Register	Interrupt Enable Register
19	Interrupt Status Register	Interrupt Status Register
20	Extended PHY Specific Control Register	
21	Receive Error Counter Register	
22	Extended Address Register	
23	Global Status Register	
24	LED Control Register	
25	Manual LED Override Register	
26	Extended PHY Specific Control 2 Register	
27	Extended PHY Specific Status Register	
28	MDI[3:0] Virtual Cable Tester Status (Page0-3); 1000BASE-T Pair Skew (Page4); 100BASE-T Pair, 1000BASE-T Pair Swap and Polarity (Page 5);	
29	Extended Address Register	

30	Calibration Override (Page3); Force Gigabit (Page7); Class A (Page11); CRC Checker result (Page12); Test Enable Control (Page16); Miscellaneous Control (Page18)
31	Reserved Register

其中:

1） reg0~15 为标准寄存器，reg16~reg31 为厂商自定义寄存器:

2） reg0~28 的页扩展由 reg22[7:0]决定，reg30 的页扩展由 reg29[4:0]决定。

3.2 寄存器操作协议

AST88E1111BI 芯片采用标准的 mdio 串行接口访问内部寄存器方式，仅实现 clause22 协议，与对标芯片一致，具体如下:

32bit preamble	Start of frame	OpCode Read=10 Write=01	5bit PHY Device Address	5bit PHY Register Address (MSB)	2bit Turn around Read=z0 Write=10	16bit data field	idle
11111111	01	10	01100	00000	z0	0001001100000000	11111111

1） Preamble：帧前缀域，为 32 个连续“1”比特;

2） Start of Frame: 以 2'b01 标识帧开始;

3） OpCode：帧操作码，2'b10 表示此帧为一读操作帧，2'b01 表示此帧为一写操作帧;

4） PHY Address：物理层芯片的地址，5bit，8 个 PHY 按 00000~00111 编址;

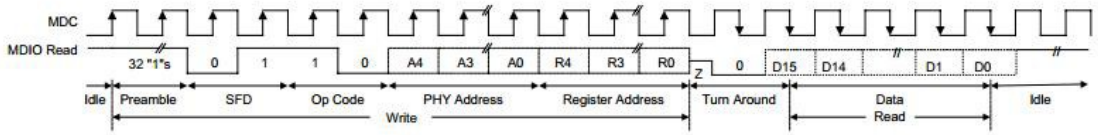
5） Reg Address：5bit，用来选择物理层芯片的 32 个寄存器中的某个寄存器的地址;

6） Turn Around：2bit，状态转换域，若为读操作，则第 1 比特时 MDIO 为高阻态，第 2 比特时由物理层芯片使 MDIO 置“0”。若为写操作，则 MDIO 仍由 MAC 层芯片控制，其连续输出“10”两个比特;

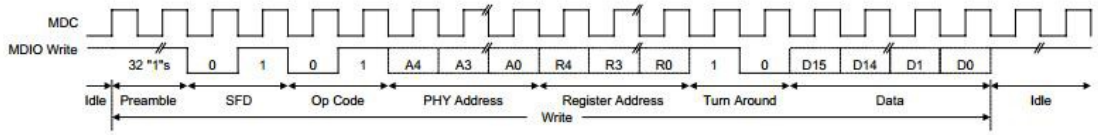
7） data：帧的寄存器的数据域，16bit，若为读操作，则为物理层送到 MAC 层的数据，若为写操作，则为 MAC 层送到物理层的数据。

支持的 MDC 时钟频率范围为 2.5MHz~8.3MHz，读写时序图如下:

2.9 Management Interface - Read Frame Structure



2.10 Management Interface - Write Frame Structure



3.3 寄存器操作方式

AST88E1111BI 芯片寄存器 reg0~15 为标准寄存器，reg16~reg31 为自定义寄存器，其中 reg0~28 的页扩展由 reg22[7:0]决定，reg30 的页扩展由 reg29[4:0]决定。

访问 reg0~28

如果访问寄存器 reg0~28，流程如下：

1） 先写 reg22[7:0]为扩展页编号，比如访问 page1 的 reg0，则写 reg22 为 16'h1；

2） 再读写对应寄存器地址即可。

访问 reg30

如果访问寄存器 reg30，流程如下：

1） 先写 reg29[4:0]为扩展页编号，比如访问 page7 的 reg30，则写 reg29 为 16'h7；

2） 再读写寄存器 reg30 即可。

3.4 详细寄存器描述

3.4.1 Copper 标准寄存器 0-15

Page 0 Register0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	RW	0x0	0x0	PHY Software Reset. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0

					automatically. The reset occurs immediately. This bit is identical to 0_1.15. 1 = PHY reset 0 = Normal operation
14	Loopback	RW	0x0	0x0	When loopback is activated, the transmitter data pre- sented on TXD is looped back to RXD internally. Link is broken when loopback is enabled. Loopback speed is determined by the mode the device is in Registers 20.6:4. In TBI Mode, this bit is set when the COL pin samples a rising edge after the RESET pin is deasserted. It is reset when the COL pin samples a Fulling edge. In all Copper modes, the loopback speed is determined by Register 20[6:4] if copper Auto-Negotiation is enabled. If copper Auto-Negotiation is disabled, the loopback speed is determined by speed set in register 0.6 and 0.13 In GMII or RGMII to Fiber Modes the loopback speed is set to 1000 Mbps. In SGMII to GMII or RGMII Modes, the loopback speed is set to SGMII Link partner advertised speed (which is the SGMII Link partners Copper Link speed) if Fiber Auto-Negotiation is enabled.' If Fiber Auto-Negotiation is disabled, the loopback speed is set from register 20 bits [6:4] Register bit 0.15 must be cleared to 0 before enabling loopback. This bit is identical to 0_1.14. 1 = Enable Loopback 0 = Disable Loopback
13	Speed[0]	RW	Descr		Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs:

					Software reset is asserted (Register 0.15) Power down (Register 0.11) transitions from power down to normal operation. Upon hardware reset this bit defaults as follows: ANEG[3:0] HWCFG_MODE[3:0] Bit 0_0.13 001x 0x00 1 001x 1x11 1 001x 1x10 1 001x 0110 1 all other configurations 0 A write to this register bit will have no effect if MODE[3:0] (either HWCF_MODE or Reg27[3:0] after a software reset) is one of the following: 1x0x, 01x1, 001x In these modes the bit will always be 0. Bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
12	Auto-Negotiation Enable	RW	Descr		Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Power down (Register 0.11) transitions from power down to normal operation. When Auto-Negotiation is enabled (0.12 = 1), the speed, Duplex, and pause capabilities are advertised in Register 4 and Register 9. If the Auto-Negotiation is disabled (0.12 = 0), then the speed and Duplex capabilities take on the settings of register bits 0.13, 0.6, and 0.8. If Register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T Full-Duplex is advertised if register 0_0.8 is set

					to 1, and 1000BASE-T Half-Duplex is advertised if 0_0.8 is set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit defaults as follows: ANEG[3:2] Bit 0.12 11 1 all other configurations 0 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
11	Power Down	RW	0x0	0x0	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0.15) and Restart Auto-Negotiation (0_0.9) are not set by the user. IEEE power down shuts down the chip except for the MAC interface if 16.3 is set to 1. If 16.3 is set to 0, then the MAC interface also shuts down. Power down also has no effect on the 125CLK output if 16.4 is set to 0. On hardware reset, bit defaults as follows: PWRUP Bit 0_0.11 1 0 0 1 This bit is identical to 1_0.11. 1 = Power down 0 = Normal operation
10	Isolate	RW	0x0	0x0	
9	Restart Auto-Negotiation	RW,SC	0x0	0x0	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0_0.9) is set. Restart Auto-Negotiation bit should be used when the Auto-Neg bit (0.12) is enabled. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Duplex Mode	RW	Descr		Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs:

					Software reset is asserted (Register 0.15) Power down (Register 0.11) transitions from power down to normal operation Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 0_0.8 00x1 1 1xxx 1 all other configurations 0 1 = Full-Duplex 0 = Half-Duplex
7	Collision Test	RW	0x0	0x0	
6	Speed[1]	RW	Desc		Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Power down (Register 0.11) transitions from power down to normal operation Upon hardware reset this bit defaults as follows: ANEG[3:0] HWCFG_MODE[3:0] Bit 0_0.6 1xxx xxxx 1 x1xx xxxx 1 xxxx xx01 1 xxxx 1x00 1 xxxx 0x11 1 xxxx 0010 1 all other configurations0 bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
5:0	Reserved				

Page 0 Register1

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	0x0	0x0	100BASE-T4.

					This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100BASE-X Full-Duplex	RO	Descr	Descr	Upon hardware reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.14 xx01 0 1x00 0 0x11 0 xx00 0 all other configurations 1 Upon software reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.14 xx01 0 1x00 0 0x11 0 all other configurations 1 1 = PHY able to perform Full-Duplex 100BASE-X 0 = PHY not able to perform Full-Duplex 100BASE-X
13	100BASE-X Half-Duplex	RO	Descr	Descr	Upon hardware reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.13 xx01 0 1x00 0 0x11 0 xx00 0 all other configurations 1 Upon software reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.13 xx01 0 1x00 0 0x11 0 all other configurations 1 1 = PHY able to perform Half-Duplex 100BASE-X 0 = PHY able to perform Half-Duplex 100BASE-X
12	10 Mbps Full-Duplex	RO	Descr	Descr	Upon hardware reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.12 xx01 0 1x00 0

					0x11 0 xx00 0 all other configurations 1 Upon software reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.12 xx01 0 1x00 0 0x11 0 all other configurations 1 1 = PHY able to perform Full-Duplex 10BASE-T 0 = PHY not able to perform Full-Duplex 10BASE-T
11	10 Mbps Half-Duplex	RO	Descr	Descr	Upon hardware reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.11 xx01 0 1x00 0 0x11 0 xx00 0 all other configurations 1 Upon software reset this bit defaults as follows: HWCFG_MODE[3:0] Bit 1.11 xx01 0 1x00 0 0x11 0 all other configurations 1 1 = PHY able to perform Half-Duplex 10BASE-T 0 = PHY not able to perform Half-Duplex 10BASE-T
10	100BASE-T2 Full-Duplex	RO	0x0	0x0	This protocol is not available. 0 = PHY not able to perform Full-Duplex
9	100BASE-T2 Half-Duplex	RO	0x0	0x0	This protocol is not available. 0 = PHY not able to perform Half-Duplex
8	Extended Status	RO	0x1	0x1	1 = Extended status information in Register 15
7	Reserved	RO	0x1	0x1	
6	MF Preamble Suppression	RO	0x0	0x0	1 = PHY accepts management frames with preamble suppressed
5	Copper Auto-Negotiation	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete

	Complete				
4	Copper remote fault	RO	0x0	0x0	Remote Fault bit is only supported in 1000BASE-T mode. 1 = Remote fault condition detected 0 = Remote fault condition not detected
3	Auto-Negotiation Ability	RO	0x1	0x1	1 = PHY able to perform Auto-Negotiation
2	Copper link status	RO	0x0	0x0	This register bit indicates whether link was lost since the last read. For the current link status, either read this register back-to-back or read Register 17_0.10 Link Real Time. 1 = Link is up 0 = Link is down
1	Jabber Detect	RO	0x0	0x0	1 = Jabber condition detected 0 = Jabber condition not detected
0	Extended Capability	RO	0x1	0x1	1 = Extended register capabilities

Page Any Register2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organization-ally Unique Identifier Bits 3:18	RO	0x0141	0x0141	Marvell® OUI is 0x005043 0000 0000 0101 0000 0100 0011 ^ ^ bit 1. ……..bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000000101000001 ^ ^ bit 3. …….bit18

Page Any Register3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	Always 000011	0x00	Organizationally Unique Identifier bits 19:24 000011 ^.....^ bit 19…….bit24
9:4	Model Number	RO	Always 001100	0x00	Model Number 88E1111 = 001100

3:0	Revision Number	RO	See Descr	See Descr	Rev Number Contact Marvell® FAEs for information on the device revision number.

Page 0 Register4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RW	0x0	0x0	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down If 1000BASE-T is advertised then the required next pages are automatically transmitted. Register 4_0.15 should be set to 0 if no additional next pages are needed. If 4_0.15 is set to 1, then Register 7_0 should be programmed with the desired value and 7_0 will be sent when 7_0.15 = 1. In GBIC mode, a Write to this register is inconsequen- tial. 1 = Advertise 0 = Not advertised
14	Ack	RO	0x0	0x0	Must be 0.
13	Remote Fault	RW	0x0	0x0	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down In GBIC mode, a Write to this register is inconsequen- tial. 1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
12	Reserved	RO	0x0	0x0	保留
11	Asymmetric Pause	RW	Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15)

					Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down In GBIC mode, a Write to this register is inconsequen- tial. Upon hardware reset this bit defaults as follows: ENA_PAUSE Bit 4_0.11 0 0 1 1 1 = Asymmetric Pause 0 = No asymmetric Pause
10	Pause	RW	Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down In GBIC mode, a Write to this register is inconsequen- tial. Upon hardware reset, this bit defaults as follows: ENA_PAUSE Bit 4_0.10 0 0 1 1 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
9	100BASE-T4	RW	0x0	0x0	0 = Not capable of 100BASE-T4
8	100BASE-TX Full-Duplex	RW	Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down In GBIC mode, a Write to this register is inconsequen- tial. If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T Full-Duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T Half-Duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8

					are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit defaults as follows: ANEG[3:0] HWCFG_MODE[3:0] Bit 4_0.8 0011 0x00 1 0011 1x11 1 11xx 0x00 1 11xx 1x11 1 all other configurations 0 1 = Advertise 0 = Not advertised
7	100BASE-TX Half-Duplex	RW	Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down In GBIC mode, a Write to this register is inconsequen- tial. If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T Full-Duplex is advertised if Register 0_0.8 is set to 1, and 1000BASE-T Half-Duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit defaults as follows: ANEG[3:0] HWCFG_MODE[3:0] Bit 4_0.7 0010 0x00 1 0010 1x11 1 11xx 0x00 1 11xx 1x11 1 all other configurations 0 1 = Advertise 0 = Not advertised
6	10BASE-TX Full-Duplex	RW	Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation

					Link goes down In GBIC mode, a Write to this register is inconsequen- tial. If Register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T Full-Duplex is advertised if Register 0_0.8 is set to 1, and 1000BASE-T Half-Duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit defaults as follows: ANEG[3:0] HWCFG_MODE[3:0] Bit 4_0.6 0001 0x00 1 0001 1x11 1 11xx 0x00 1 11xx 1x11 1 all other configurations 0 1 = Advertise 0 = Not advertised
5	10BASE-TX Half-Duplex	RW	Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down In GBIC mode, a Write to this register is inconsequen- tial. If Register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T Full-Duplex is advertised if Register 0_0.8 is set to 1, and 1000BASE-T Half-Duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit defaults as follows: ANEG[3:0] HWCFG_MODE[3:0] Bit 4_0.5 0000 0x00 1 0000 1x11 1 11xx 0x00 1

					11xx 1x11 1 all other configurations 0 1 = Advertise 0 = Not advertised
4:0	Selector Field	RO	0x1	0x1	Selector Field mode 00001 = 802.3

Page 0 Register5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page receives Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link Partner has not received link code word
13	Remote Fault	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault
12	Technology Ability	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 12
11	Asymmetric Pause	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
10	Pause	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 10 1 = Link partner is capable of symmetric pause

					operation 0 = Link partner is not capable of symmetric pause operation
9	100BASE-T4	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable
8	100BASE-TX Full-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 8 1 = Link partner is 100BASE-TX Full-Duplex capable 0 = Link partner is not 100BASE-TX Full-Duplex capable
7	100BASE-TX Half-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 7 1 = Link partner is 100BASE-TX Half-Duplex capable 0 = Link partner is not 100BASE-TX Half-Duplex capable
6	10BASE-TX Full-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 6 1 = Link partner is 10BASE-T Full-Duplex capable 0 = Link partner is not 10BASE-T Full-Duplex capable
5	10BASE-TX Half-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 5 1 = Link partner is 10BASE-T Half-Duplex capable 0 = Link partner is not 10BASE-T Half-Duplex capable
4:0	Selector Field	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received. Selector Field Received Code Word Bit 4:0

Page 0 Register6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved				
4	Parallel Detection Fault	RO,LH	0x0	0x0	6_0.3 is set when a base page is received and the received link control word has bit 15 set to 1. The bit is cleared when link goes down. 1 = A fault has been detected via the Parallel Detection function 0 = A fault has not been detected via the Parallel Detection function
3	Link Partner Next page Able	RO	0x0	0x0	Register 6_0.3 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	Local Next Page Able	RO	Always 1	Always 1	1 = Local Device is Next Page able
1	Page Received	RO,LH	0x0	0x0	Register 6_0.1 is set when a valid page is received. 1 = A New Page has been received 0 = A New Page has not been received
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	This bit is set when the device receives 3 matching FLP bursts and the Auto-Negotiation is enabled in register 0.0.12 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Page 0 Register7

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RW	0x0	0x0	A write to register 7_0 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Transmit Code Word Bit 15
14	Reserved				This bit must be read and left unchanged when performing a write.
13	Message Page	RW	0x1	0x1	Transmit Code Word Bit 13

	Mode				
12	Acknowledge2	RW	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	R0	0x0	0x0	Transmit Code Word Bit 11. This bit is internally set to the opposite value each time a page is received
10:0	Message Unformatted Field	RW	0x1	0x1	Transmit Code Word Bit 10:0

Page 0 Register8

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	The register is loaded only when a next page is received from the link partner. It is cleared each time the link goes down. Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page Mode	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12
11	Toggle	R0	0x0	0x0	Received Code Word Bit 11
10:0	Message Unformatted Field	RO	0x0	0x0	Received Code Word Bit 10:0

Page 0 Register9

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Test Mode	RW	0x0	0x0	After exiting the test mode, hardware reset or software reset (Register 0.15) should be issued to ensure normal operation. A restart of Auto-Negotiation will clear these bits. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 101, 110, 111 = Reserved

					The transmitting clock which is synchronous to the test data is sourcing from the RX_CLK pin for jitter testing in test modes 2 and 3.
12	MASTER/SLAVE Manual Configuration Enable	RW	Descr	Retain	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 9_0.12 xx1x 0 all other configurations 1 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration
11	MASTER/SLAVE Configuration Value	RW	Descr	Retain	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Register 9_0.11 is ignored if Register 9_0.12 is equal to 0. Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 9_0.11 xxx1 0 all other configurations 1 1 = Manual configure as MASTER 0 = Manual configure as SLAVE
10	Port Type	RW	Descr	Retain	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0.11) transitions from power down to normal operation

					Link goes down Register 9_0.10 is ignored if Register 9_0.12 is equal to 1. Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 9_0.10 xxx1 0 all other configurations 1 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)
9	1000BASE-T Full Duplex	RW	Descr	Retain	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 9_0.9 1xxx 1 all other configurations 0 1 = Advertise 0 = Not advertised
8	1000BASE-T Half Duplex	RW	0x0		Always 0
7:0	Reserved				

Page 0 Register10

Bits	Field	Mode	HW Rst	SW Rst	Description
15	MASTER/SLAVE Configuration Fault	RO,LH	0x0	0x0	This register bit will clear on read and restart autoneg It is set to 0 when Auto-Negotiation is off 1 = MASTER/SLAVE configuration fault detected 0 = No MASTER/SLAVE configuration fault detected
14	MASTER/SLAVE Configuration Resolution	RO	0x0	0x0	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration

					resolved to SLAVE
13	Local Receiver Status	RO	0x0	0x0	1 = Local Receiver OK 0 = Local Receiver is Not OK
12	Remote Receiver Status	RO	0x0	0x0	1 = Remote Receiver OK 0 = Remote Receiver Not OK
11	Link Partner 1000BASE-T Full-Duplex Capability	RO	0x0	0x0	1 = Link Partner is capable of 1000BASE-T Full-Duplex 0 = Link Partner is not capable of 1000BASE-T Full- Duplex
10	Link Partner 1000BASE-T Half-Duplex Capability	RO	0x0	0x0	1 = Link Partner is capable of 1000BASE-T Half-Duplex 0 = Link Partner is not capable of 1000BASE-T Half- Duplex
9:8	Reserved	RO	0x0	0x0	
7:0	Idle Error Count	RO	0x0	0x0	MSB of Idle Error Counter These register bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and will not roll over.

Page Any Register11

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved				

Page Any Register12

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved				

Page Any Register13

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved				

Page Any Register14

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved				

Page Any Register15

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000BASE-X Full-Duplex	RO	0x0	0x0	This bit is set to 1 when mode is one of these: 0011, 0110, 0111, 1000 This bit is also set to 1 if auto Fiber/copper mode is on when mode is one of these: 1001, 1011, 1101, 1111 Any other mode/auto-Fiber-copper combination, this bit is set to 0 1 = 1000 BASE-X Full-Duplex capable 0 = not 1000 BASE-X Full-Duplex capable
14	1000BASE-X Half-Duplex	RO	0x0	0x0	always 0
13	1000BASE-T Full-Duplex	RO	0x1	0x1	This bit is set to 1 when mode is one of these: 0000, 0100, 1000, 1001, 1011, 1101, 1111 Any other mode, this bit is set to 0 1 = 1000 BASE-X Full-Duplex capable 0 = not 1000 BASE-X Full-Duplex capable
12	1000BASE-T Half-Duplex	RO	0x0	0x0	always 0
11:0	Reserved				

3.4.2 Fiber 标准寄存器 reg0-15

Page 0 Register0

Bits	Field	Mode	Description
15	RESET	RW SC	PHY Software Reset. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs

			immedi- ately. This bit is identical to 0_0.15. 1 = PHY reset 0 = Normal operation
14	PCS LOOPBACK	RW	When loopback is activated, the transmitter data pre-sented on TXD is looped back to RXD internally. Link is broken when loopback is enabled. Loopback speed is determined by the mode the device is in Registers 20.6:4. In all Copper modes, the loopback speed is determined by Register 20[6:4] if copper Auto-Negotiation is enabled. If copper Auto-Negotiation is disabled, the loopback speed is determined by speed set in register 0.6 and 0.13 In GMII or RGMII to Fiber Modes the loopback speed is set to 1000Mbps In SGMII to GMII or RGMII Modes, the loopback speed is set to SGMII Link partner advertised speed (which is the SGMII Link partners Copper Link speed) if Fiber Auto-Negotiation is enabled. This bit is identical to 0_0.14. 1 = Enable Loopback 0 = Disable Loopback
13	speed select(LSB)	RO	bit 6,13 10 = 1000 Mbps
12	自协商使能	RW	Changes to this bit are disruptive to the normal opera- tion; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0.11) transitions from power down to normal operation Fiber link goes down. This bit enables

			Auto-Negotiation on the Fiber interface in all configurations where the ser- des is used. Upon hardware reset this bit defaults as follows: MODE [3:0] ANEG[3:2] Bit 0.12 x000 xx 1 x110 xx 1 0100 xx 1 xx11 11 1 all other configurations 0 When this bit gets set/reset, Auto-Negotiation is restarted (bit 1.0.9 is set to 1) 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
11	power down	RW	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0.15) and Restart Auto-Negotiation (0_1.9) are not set by the user. IEEE power down shuts down the chip except for the MAC interface if 16.3 is set to 1. If 16.3 is set to 0, then the MAC interface also shuts down. Power down also has no effect on the 125CLK output if 16.4 is set to 0. On hardware reset, bit defaults as follows: PWRUP Bit 1_0.11 1 0 0 1 This bit is identical to 0_0.11. 1 = Power down 0 = Normal operation
10	isolate	RW	
9	restart auto-nego	RW SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0_1.9) is set. The bit is set when Auto-Negotiation is Enabled or Dis- abled in 1.0.12 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Fiber Duplex	RW	

7	collision test	RW	
6	speed select (MSB)	RO	bit 6, 13 10 = 1000 Mbps
5:0	保留		

Page 0 Register1

Bits	Field	Mode	Description
15	100BASE T4	RO	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100 X Full Duplex	RO	0 = PHY not able to perform Full-Duplex 100BASE-X
13	100 X Half Duplex	RO	0 = PHY not able to perform Full-Duplex 100BASE-X
12	10 Full Duplex	RO	0 = PHY not able to perform Full-Duplex 10BASE-T
11	10 Half Duplex	RO	0 = PHY not able to perform Half-Duplex 10BASE-T
10	100 T2 Half Duplex	RO	This protocol is not available. 0 = PHY not able to perform Full-Duplex
9	100 T2 Full Duplex	RO	This protocol is not available. 0 = PHY not able to perform Half-Duplex
8	extend status	RO	1 = Extended status information in Register 15
7	保留	RO	
6	MF preamble suppression	RO	1 = PHY accepts management frames with preamble suppressed
5	Fiber auto-nego complete	RO	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete Bit is not set when link is up due of Fiber Auto-Negotia- tion Bypass or if Auto-Negotiation is disabled.
4	Fiber remote fault	RO LH	1 = Remote fault condition detected 0 = Remote fault condition not detected This bit is always 0 in SGMII to Copper and SGMII to GMII or RGMII Modes.
3	auto-nego ability	RO	1 = PHY able to perform Auto-Negotiation
2	Fiber link status	RO LL	This register bit indicates when link was lost since the last read. For the current link status, either read this reg- ister back-to-back or read Register 17_1.10 Link Real Time. 1 = Link is up 0 = Link is down
1	保留	RO	

0	extend capability	RO	1 = Extended register capabilities

Page 0 Register 2/3

Bits	Filed	Mode	Description
15~0	PHY ID	RO	

Page 0 Register 4 Fiber mode

Bits	Field	Mode	Description
15	Next page	RW	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
14	保留	RW	
13:12	远程故障	RW	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Device has no ability to detect remote fault. 00 = No error, link OK（Default） 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	保留	RW	
8:7	pause	RW	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0.11) transitions from

			power down to normal operation Link goes down Upon hardware reset, this bit defaults as follows: ENA_PAUSE Bits 4_1.8:7 0 00 1 11 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.
6	半双工	RW	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 4_1.6 x1xx 1 all other configurations0 1 = Advertise 0 = Not advertised
5	全双工	RW	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down Upon hardware reset this bit defaults as follows: ANEG[3:0] Bit 4_1.5 1xxx 1 all other configurations 0
4:0	保留		1 = Advertise 0 = Not advertised

Page 0 Register 4 SGMII PHY mode

Bits	Filed	Mode	Description
15	Copper link status	RO	0 = Link is Not up on the Copper Interface 1 = Link is UP on the Copper Interface
14:13	保留		
12	Copper 双工状态	RO	0 = Copper Interface Resolved to Half-Duplex 1 = Copper Interface Resolved to Full-Duplex
11:10	Copper 速率	RO	00 = Copper Interface speed is 10 Mbps 01 = Copper Interface speed is 100 Mbps 10 = Copper Interface speed is 1000 Mbps 11 = Reserved
9:0	保留		

Page 0 Register 4 SGMII MAC mode

Bits	Filed	Mode	Description
15:0	保留		

Page 0 Register 5 Fiber mode

Bits	Filed	Mode	Description
15	Next page	RO	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
14	ACK		Register bit is cleared when link goes down and loaded when a base page is received. Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:12	Remote fault	RO	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 13:12 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error

11:9	保留	RO	
8:7	pause	RO	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 8:7 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.
6	半双工	RO	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word bit 6 1 = Link partner capable of 1000BASE-X Half-Duplex. 0 = Link partner not capable of 1000BASE-X Half-Duplex.
5	全双工	RO	Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word bit 5 1 = Link partner capable of 1000BASE-X Full-Duplex. 0 = Link partner not capable of 1000BASE-X Full-Duplex.
4:0	保留	RO	

Page 0 Register 5 SGMII MAC mode

Bits	Filed	Mode	Description
15	Copper link status	RO	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Copper Link is up on the link partner 0 = Copper Link is not up on the link partner
14	ACK	RO	Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13	保留		
12	Copper 双工状态	RO	Register bit is cleared when link goes down and loaded when a base page is received

			Received Code Word Bit 12 1 = Copper Interface on the Link Partner is capable of Full-Duplex 0 = Copper Interface on the link partner is capable of Half-Duplex
11:10	Copper 速率	RO	Register bits are cleared when link goes down and loaded when a base page is received Received Code Word Bit 11:10 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = reserved
9:0	保留		

Page 0 Register 5 SGMII PHY mode

Bits	Filed	Mode	Description
15	保留		
14	ACK	RO	Acknowledge Register bit is cleared when link goes down and loaded when a base page is received. Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:0	保留		

Page 0 Register 6

Bits	Filed	Mode	Description
15:4	保留		
3	link partner next page able	RO	In SGMII to Copper, SGMII to RGMII, GBIC and Legacy GBIC Modes this bit is always 0. In all the other modes register 6_1.3 is set when a base page is received and the received link control word has bit 15 set to 1. The bit is cleared when link goes down. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	local next page able	RO	1 = Local Device is Next Page able
1	page received	RO	Register 6_1.1 is set when a valid page is

		LH	received. 1 = A New Page has been received 0 = A New Page has not been received
0	link partner auto-nego able	RO	This bit is set when there is sync status, the Fiber receiver has received 3 non-zero matching valid config- uration code groups and Auto-Negotiation is enabled in register 1.0.12 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Page 0 Register 7

Bits	Filed	Mode	Description
15	Next page	RW	A write to register 7_1 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Transmit Code Word Bit 15
14	保留		
13	message page mode	RW	Transmit Code Word Bit 13
12	ack2	RW	Transmit Code Word Bit 12
11	Toggle	RO	Transmit Code Word Bit 11. This bit is internally set to the opposite value each time a page is received.
10:0	message/ unformatted field	RW	Transmit Code Word Bit 10:0

Page 0 Register 8

Bits	Filed	Mode	Description
15	Next page	RO	The register is loaded only when a next page is received from the link partner. It is cleared each time the link goes down. Received Code Word Bit 15
14	ACK	RO	Received Code Word Bit 14
13	message page mode	RO	Received Code Word Bit 13
12	ACK2	RO	Received Code Word Bit 12
11	Toggle	RO	Received Code Word Bit 11
10:0	message/ unformatted field	RO	Received Code Word Bit 10:0

3.4.3 非标准寄存器 reg16-31

Page 0 Register 16 PHY Specific Control Register

Bits	Filed	Mode	Description
15:5	保留		
4	Disable 125CLK	RW	Changes to this bit are disruptive to the normal opera- tion; therefore, any changes to these registers must be followed by a software reset to take effect. Upon hardware reset this bit defaults as follows DIS_125 Bit 16.4 0 0 1 1 1 = 125CLK low 0 = 125CLK toggle
3:2	保留		
1	Polarity Reversal	RW	If polarity is disabled, then the polarity is forced to be normal in 10BASE-T. 1 = Polarity Reversal Disabled 0 = Polarity Reversal Enabled
0	DisableJabber	RW	Jabber has effect only in 10BASE-T Half-Duplex mode. 1 = Disable jabber function 0 = Enable jabber function

Page 0 Register17 PHY Specific Status Register-Copper

Bits	Filed	Mode	Description
15:14	速度状态	RO	These status bits are valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotia- tion is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	双工状态	RO	This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is com- pleted or Auto-Negotiation is disabled. 1 = Full-Duplex

			0 = Half-Duplex
12	页接收	RO LH	1 = Page received 0 = Page not received
11	速度和双工状态输出使能	RO	When Auto-Negotiation is not enabled 17_0.11 = 1. 1 = Resolved 0 = Not resolved (If bit 27.11 is 1, then this bit will be 0.)
10	链路实时 OK	RO	1 = Link up 0 = Link down
9:7	线缆长度（1g only）	RO	
6	MDIX 状态	RO	This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is com- pleted or Auto-Negotiation is disabled. This bit is 0 or 1 depending on what is written to 16.6:5 in manual config- uration mode. Register 16.6:5 are updated with software reset. 1 = MDIX 0 = MDI
5	Downshift Status	RO	
4	Copper Energy Detect Status	RO	
3	发送 Pause 使能	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is com- pleted or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disable
2	接收 Pause 使能	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is com- pleted or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
1	极性实时状态	RO	1 = Reversed 0 = Normal
0	Jabber 实时状态	RO	1 = Jabber 0 = No jabber

Page 1 Register 17 PHY Specific Status Register-Fiber

Bits	Filed	Mode	Description
15:14	速度状态	RO	These status bits are valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotia- tion is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	双工状态	RO	This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is com- pleted or Auto-Negotiation is disabled. 1 = Full-Duplex 0 = Half-Duplex
12	页接收	RO LH	1 = Page received 0 = Page not received
11	速度和双工状态输出使能	RO	When Auto-Negotiation is not enabled or mode is 0001 or 0101 17_1.11 = 1. 1 = Resolved 0 = Not resolved If bit 27.11 is 1, then this bit will be 0.
10	链路实时 OK	RO	1 = Link up 0 = Link down
9:4	保留	RO	
3	发送 Pause 使能	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is com- pleted or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disable
2	接收 Pause 使能	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used

			by the device. This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is com- pleted or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
1:0	保留	RO	

Page 0 Register 18 Interrupt Enable Register -Copper

Bits	Filed	Mode	Description
15	自协商错误中断使能	RW	1 = Interrupt enable 0 = Interrupt disable
14	速度改变中断使能	RW	1 = Interrupt enable 0 = Interrupt disable
13	双工改变中断使能	RW	1 = Interrupt enable 0 = Interrupt disable
12	页接收中断使能	RW	1 = Interrupt enable 0 = Interrupt disable
11	自协商完成中断使能	RW	1 = Interrupt enable 0 = Interrupt disable
10	链路状态改变中断使能	RW	1 = Interrupt enable 0 = Interrupt disable
9	字符错误中断使能	RW	
8	False Carrier 中断使能	RW	
7	FIFO 上下溢中断使能	RW	
6	MDIX 改变中断使能	RW	1 = Interrupt enable 0 = Interrupt disable
5	Downshift 中断使能	RW	
4	Energy Detect 中断使能	RW	
3	保留		
2	DTE 功耗检测状态中断使能	RW	
1	极性改变中断使能	RW	1 = Interrupt enable 0 = Interrupt disable
0	Jabber 中断使能	RW	1 = Interrupt enable 0 = Interrupt disable

Page 1 Register 18 Interrupt Enable Register-Fiber

Bits	Filed	Mode	Description
15	保留	RO	
14	速度改变中断使能	RW	1 = Interrupt enable 0 = Interrupt disable
13	双工改变中断使能	RW	1 = Interrupt enable 0 = Interrupt disable
12	页接收中断使能	RW	1 = Interrupt enable 0 = Interrupt disable
11	自协商完成中断使能	RW	1 = Interrupt enable 0 = Interrupt disable
10	链路状态改变中断使能	RW	1 = Interrupt enable 0 = Interrupt disable
9:0	保留	RO	

Page 0 Register 19 Interrupt Status Register

Bits	Filed	Mode	Description
15	自协商错误中断使能	RO LH	An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed. 1 = Auto-Negotiation 0 = No Auto-Negotiation
14	速度改变中断使能	RO LH	1 = Speed changed 0 = Speed not changed
13	双工改变中断使能	RO LH	1 = Duplex changed 0 = Duplex not changed
12	页接收中断使能	RO LH	1 = Page received 0 = Page not received
11	自协商完成中断使能	RO LH	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	链路状态改变中断使能	RO LH	1 = Link status changed 0 = Link status not changed
9	字符错误中断使能	RO LH	
8	False Carrier 中断使能	RO LH	
7	FIFO 上下溢中断使能	RO LH	
6	MDIX 改变中断使能	RO LH	1 = Crossover changed 0 = Crossover not changed
5	Downshift 中断使能	RO LH	
4	Energy Detect 中断使	RO LH	

	能		
3	保留	RO LH	
2	DTE 功耗检测状态中断使能	RO LH	
1	极性改变中断使能	RO LH	1 = Polarity Changed 0 = Polarity not changed
0	Jabber 中断使能	RO LH	1 = Jabber 0 = No jabber

Page 1 Register 19 Fiber

Bits	Filed	Mode	Description
15:0	含义同寄存器 18，区别在于本寄存器表示中断状态	RO LH	

Page 0 Register 20 Extended PHY Specific Control Register

Bits	Filed	Mode	Description
15:8	保留		
7	RGMII Receive Timing Control	RW	Changes to this bit are disruptive to the normal opera- tion; hence, any change to this register must be followed by software reset to take effect. 1 = Add delay to RX_CLK for RXD Outputs See“RGMII Delay Timing for different RGMII Modes” on page 218.
6:2	保留		
1	RGMII Transmit Timing Control	RW	Changes to this bit are disruptive to the normal opera- tion; hence, any change to this register must be followed by software reset to take effect. 1 = Add delay to GTX_CLK for TXD Outputs See“RGMII Delay Timing for different RGMII Modes” on page 218.
0	保留		

Page 0 Register 21 Receive Error Counter Register

Bits	Filed	Mode	Description
15:0	Receive Error Count	RO LH	Counter will peg at 0xFFFF and will not roll over. Both False carrier and symbol errors are reported. The following modes of operation have the receive errors

			reported from Fiber media. 0011,0111,0110 and 1110. Copper media receive errors are reported in the remaining modes of operation.

Page 0 Register 22 Extended Address

Bits	Filed	Mode	Description
15:8	保留		
7:0	Page select for registers 0 to 28	RW	Register bits 22.7:0 are used for Fiber/copper register identity selection. 0x00 = Selects copper banks of registers 0, 1, 4, 5, 6, 7, 8, 17, 18, 19. 0x01 = Selects Fiber banks of registers 0, 1, 4, 5, 6, 7, 8, 17, 18, 19. At the same time register 22.7:0 also selects the VCT pair for results to be read from register 28. 0x03 = MDI pair 3 0x02 = MDI pair 2 0x01 = MDI pair 1 0x00 = MDI pair 0 See Table 94 for details. Reg22[7:0] = 01 when Reg27[3:0] is either 0110, 1110, 0011 or 0111 and Reg22[7:0] = 00 when Reg27[3:0] is either 1001, 1101, 1011, 1111 and reg27[15] = 1. When modes is either 0000, 0010, 0100, 1000, 1010, or 1100 and Reg27[15] = 0 and Reg27[9] = 0 then Reg22[7:0] will be 0x00 or 0x01 depends on if the phy is resolved to Fiber or copper. If Reg27[15] or Reg27[9] = 1, writing 0x01 to Reg22[7:0] for Fiber registers banks accesses and writing 00 to Reg22[7:0] for Copper registers banks accesses.

Page 0 Register 23 Global Status Register

Bits	Filed	Mode	Description
15:1	保留		
0	Port 0 Interrupt	RO	1 = Interrupt on Port 0 = No Interrupt on Port

			Bit will stay high until active interrupts bits cleared on a read of register 19 of the corresponding port.

Page 0 Register 24 LED Control Register

Bits	Filed	Mode	Description
15	Disable LED	RW	1 = Disable 0 = Enable
14:12	Pulse stretch duration	RW	000 = no pulse stretching 001 = 21 ms to 42ms 010 = 42 ms to 84ms 011 = 84 ms to 170ms 100 = 170 ms to 340ms 101 = 340 ms to 670ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s
11	Force Interrupt	RW	1 = Force INTn pin to assert 0 = Normal operation
10:8	Blink Rate	RW	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
7	LED_Duplex Control	RW	See Bit 2
6	LED_TX Con- trol (LSB)	RW	bit 0,6 See section 2.22.2.3 for more details 00 = Transmit activity - solid on 01 = Transmit or receive activity - solid on 10 = Link and no activity - solid on. Transmit or receive activity - blink 11 = Transmit or receive activity - blink
5:3	LED_LINK Control	RW	000 = Direct LED mode 011 = Master/Slave LED mode 001, 010, 100, 111, all other values = see datasheet section Combined Link LED modes
2	LED_ DUPLEX Control	RW	Bit 7,2 - LED DUPLEX Behavior 0 -- Low = Full-Duplex, High = Half-Duplex, Blink = Col- lision 1 -- Low = Full-Duplex, High = Half-Duplex 10 -- Low = Fiber Link Up, High = Fiber Link Down 11 -- Reserved
1	LED_RX Control	RW	See section 2.22.2.3 for more information. 1 = Receive activity/Link

			0 = Receive activity
0	LED_TX control (MSB)	RW	See bit 6

Page 0 Register 25 LED Override Register

Bits	Filed	Mode	Description
15:14			
13:12	保留		
11:10	LED_ DUPLEX	RW	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
9:8	LED_ LINK10	RW	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
7:6	LED_ LINK100	RW	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
5:4	LED_ LINK1000	RW	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
3:2	LED_RX	RW	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
1:0	LED_TX	RW	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink

			10 = LED Off 11 = LED On

Page 0 Register 26 Extended PHY Specific Control 2 Register

Bits	Filed	Mode	Description
15:0	保留		

Page 0 Register 27 Extended PHY Specific Status Register

Bits	Filed	Mode	Description
15:11	保留		
10	Interrupt Polarity	RW	Changes to this bit are disruptive to the normal opera- tion; hence, any changes to these registers must be fol- lowed by software reset to take effect. Default takes the value of INT_POL. 1 = INT active low 0 = INT active high
9:4	保留		
3:0	HWCFG_MODE	RW	Changes to these bits are disruptive to the normal oper- ation; hence, any changes to these registers must be followed by software reset to take effect. Upon hardware reset Register 27.3:0 defaults to the value in HWCFG_MODE[3:0]. 0100 = SGMII without Clock with SGMII Auto-Neg to copper 0110 = RGMII to SGMII 1110 = GMII to SGMII 0011 = RGMII to Fiber 0111 = GMII to Fiber 1011 = RGMII to Copper 1111 = GMII to copper Others = Reserved

Page 0~3 Register 28 Virtual Cable Tester Status Register

Btis	Filed	Mode	Description
15:0	保留		

Page 4 Register 28 1000BASE-T Pair Skew Register

Bits	Filed	Mode	Description
15:0	保留		

Page 5 Register 28 1000Base-T Swap and Polarity Status Register

Bits	Filed	Mode	Description
15:6	保留		
5	C,D crossover	RO	1 = Channel C received on MDI[2]± Channel D received on MDI[3]± 0 = Channel D received on MDI[2]± Channel C received on MDI[3]±
4	A,B crossover	RO	1 = Channel A received on MDI[0]± Channel B received on MDI[1]± 0 = Channel B received on MDI[0]± Channel A received on MDI[1]±
3	Pair 7,8 (MDI[3]±) Polarity	RO	1 = Negative 0 = Positive
2	Pair 4,5 (MDI[2]±) Polarity	RO	1 = Negative 0 = Positive
1	Pair 3,6 (MDI[1]±) Polarity	RO	1 = Negative 0 = Positive
9	Pair 1,2 (MDI[0]±) Polarity	RO	1 = Negative 0 = Positive

Page Any Register 29 Extended Address

Bits	Filed	Mode	Description
15:5	保留		These bits must be read and left unchanged when Performing a write
4:0	Page select		00000 = no register 30 page access or Page 0 of regis- ter 30 00011 = Select Page 3 of register 30 00111 = Select Page 7 of register 30 01100 = Select Page 12 of register 30 10000 = Select Page 16 of register 30 10010 = Select Page 18 or register 30

Page 3 Register 30 Cailbration Override

Bits	Filed	Mode	Description
15:0	保留		

Page 7 Register 30 Force Gigabit Mode

Bits	Filed	Mode	Description
15:0	保留		

Page 11 Register 30 Transmitter Type

Bits	Filed	Mode	Description
15:0	保留		

Page 12 Register 30 CRC checker result

Bits	Filed	Mode	Description
15:8	Frame count	RO	Frame count is stored in these bits. 00000000 = No frame counted 11111111 = Maximum number of frames counted The counter does not clear on a read command. To clear the CRC error counter, disable the crc_checker (Register 30_16.15 = 0).
7:0	CRC error count	RO	Error counter is stored in these bits. 00000000 = No frame counted 11111111 = Maximum number of frame counted The counter does not clear on a read command. To clear the CRC error counter, disable the crc_checker (Register 30_16.15 = 0).

Page 16 Register 30 Test Enable Control

Bits	Filed	Mode	Description
15:1	保留		
0	Enable CRC checker	RW	1 = Enable CRC checker 0 = Disable CRC checker, clear frame counter and CRC error counter (Register 30_1215:0 = 0x0000)

Page 18 Register 30 Miscellaneous Control

Bits	Filed	Mode	Description
15:0	保留		

Page 0 Register 31 Reserved Registers

Bits	Filed	Mode	Description
15:0	保留		

第四章 电气特性

4.1 极限参数

模拟电压 (VDDH)……-0.3V~+2.75V
MAC 接口 IO 电压 (VDDO)……-0.3V~3.63V
其他 IO 电压 (VDDOX)……-0.3V~+3.63V
数字电压 (DVDD)……-0.3V~+1.21V
结点温度（Tj）……125℃
贮存温度范围（Tstg）……-65℃~150℃

注意，超出上述绝对最大额定值可能会导致器件永久性损坏。这只是额定最值，不表示在这些条件下，或者任何其它超出本技术规范操作部分所示规格的条件下，器件能够正常工作。长期在绝对最大额定值条件下工作会影响器件的可靠性。

4.2 推荐工作条件

模拟电压 (VDDH)……2.375V~2.625V;
数字电压 (DVDD)……1.05V~1.15V;
MAC 接口 IO 电压 (VDDO)……1.7V~1.9V/2.375~2.625V/3.135V~3.465V;
其他 IO 电压 (VDDOX)……1.7V~1.9V/2.375~2.625V/3.135V~3.465V;
工作环境温度（T_A）（工业级）…… -40℃~85℃;
工作环境温度（T_A）（企军级）…… -55℃~125℃;

4.3 直流电气属性

4.3.1 功耗参数

注：参数 DVDDIO=VDDO+VDDOX 两者之和测得的数据结果

条件	电压域	电流（mA）
GMII over 1000BASE-T with traffic	2.5V（VDDH）	103
	DVDDIO（1.8/2.5/3.3）	12/20/27
	1.1V（DVDD）	114
RGMII over 1000BASE-T with traffic	2.5V（VDDH）	103
	DVDDIO（1.8/2.5/3.3）	16/25/35
	1.1V（DVDD）	115
SGMII over 1000BASE-T with traffic	2.5V（VDDH）	126
	DVDDIO（1.8/2.5/3.3）	2/2/2
	1.1V（DVDD）	197
GMII over 1000BASE-X with traffic	2.5V（VDDH）	34
	DVDDIO（1.8/2.5/3.3）	11/18/25
	1.1V（DVDD）	116
RGMII over 1000BASE-X with traffic	2.5V（VDDH）	34
	DVDDIO（1.8/2.5/3.3）	13/20/28
	1.1V（DVDD）	116
RGMII over 100BASE-TX with traffic	2.5V（VDDH）	34
	DVDDIO（1.8/2.5/3.3）	6/9/15
	1.1V（DVDD）	46
RGMII over 10BASE-T with traffic	2.5V（VDDH）	44
	DVDDIO（1.8/2.5/3.3）	4/6/7
	1.1V（DVDD）	37

4.3.2 直流电气参数

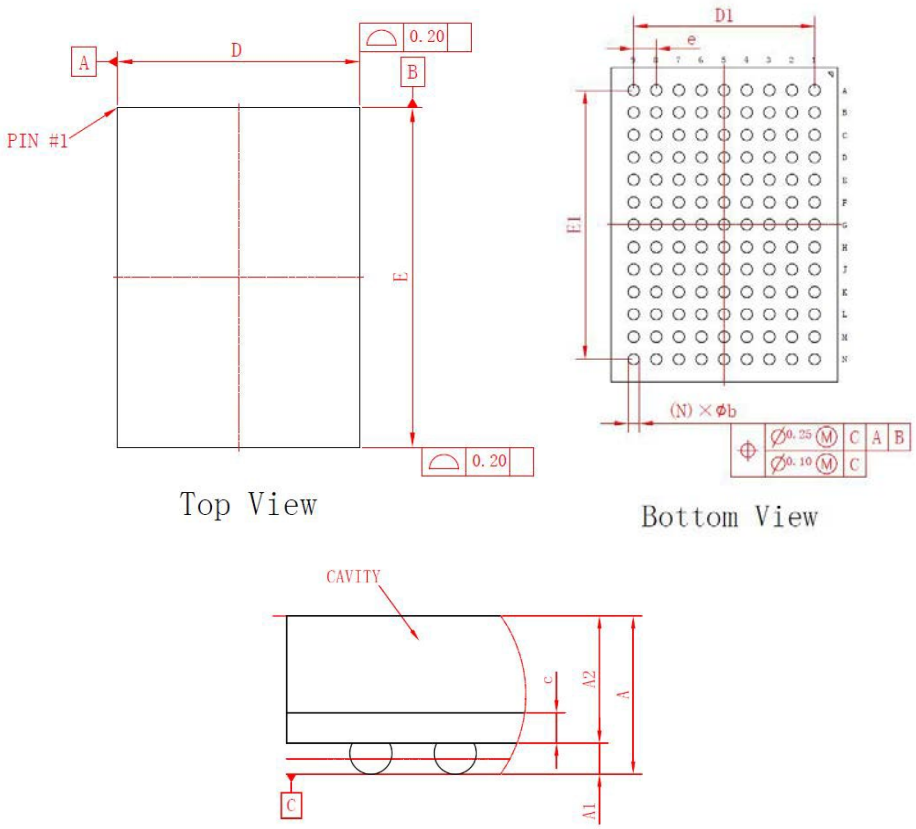
RGMII 输入逻辑电平	高	VDDO*0.7	V
	低	VDDO*0.3	V
RGMII 输出逻辑电平	高	VDDO*0.7	V
	低	VDDO*0.3	V
MDC,MDIO,125CLK,RESETn,INTn 输入逻辑电平	高	VDDOX*0.7	V
	低	VDDOX*0.3	V
MDC,MDIO,125CLK,RESETn,INTn 输出逻辑电平	高	VDDOX*0.7	V
	低	VDDOX*0.3	V
其他数字 IO 输入逻辑电平	高	2.0	V
	低	0.8	V
其他数字 IO 输出逻辑电平	高	2.0	V

	低	0.8	V

第五章 封装信息

5.1 封装形式及外形尺寸

AST88E1111BI 芯片的封装形式为 TFBGA 117-pin，尺寸描述如下图:

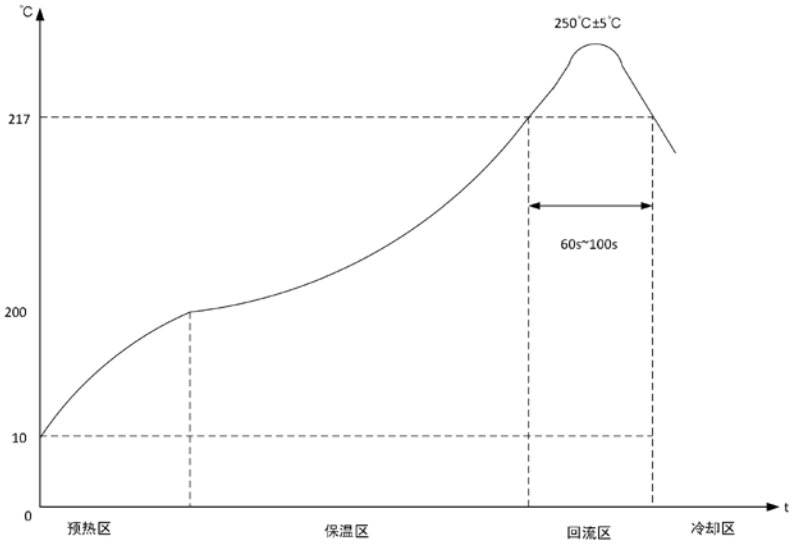


封装尺寸信息如下表:

符号	单位为毫米		
	最小	公称	最大
A	1.62	---	1.980
A1	0.320	---	0.57
A2	1.17	---	1.560
c	0.320	0.360	0.400
D	9.900	10.000	10.100
E	13.900	14.000	14.100
D1	---	8.000	---
E1	---	12.000	---
e	---	1.000	---
b	0.450	0.500	0.72

表 6 芯片封装尺寸

5.2 推荐焊装工艺曲线



步骤	条件
预热区	
温度	150℃~200℃
40℃升至 120℃的时间	60s~100s
温变率	温升率最大 3℃/s
保温区	
保温区温度	200℃~217℃
温变率	最大 3℃/s
回流区	
回 流 时 间	60s~100s
回流区温度	217℃
峰值温度	250℃±5℃
峰值温度保持时间	30s~40s
冷却时间	
冷却时间	降温率最大-6℃/s

第六章 订货信息

型号	质量等级	工作温度	封装
AST88E1111BI	工业级	-45 ~ 85°C	TF-BGA 117 pin

差异列表

项目	AST88E1111BI	Marvell 88E1111
DVDD 电源域	Typ：1.1v	Typ：1.0v 或 1.2v
VDDOX 电源域	Typ：1.8v 或 2.5v 或 3.3v	TYP:2.5v
VDDO 电源域	Typ：1.8v 或 2.5v 或 3.3v	TYP:2.5v
RTBI/TWSI/TBI/JTAG 接口	不支持	支持
变压器方案	中心抽头接地或者 2.5v 不抽取电流	中心抽头需接 2.5v 需要抽取电流
MDI 口端口	内置端接 100 欧姆差分阻抗	外部端接 100 欧姆差分阻抗
HBM ESD 防护	3000v	2000v
功耗	芯片最大 0.6W 变压器中心抽头 0W	芯片最大 0.8W 变压器中心抽头最大 0.5W
工作温度	-40~85℃（工业级）	-40~85℃

重点说明：

1. VDDO（引脚 K1/C2/B4）决定 R/G/MII 接口电压。
2. VDDOX(引脚 K9/L2)决定 MDC/MDIO/INTn/125CLK/RESETn/COMA 接口电压。MDIO/INTn/RESETn/COMA 的上拉电阻需要上拉到 VDDOX。
3. DVDD 电源域建议使用1.1V，经验证1.0V 或 1.2V 在高低温下也均可正常使用。